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NETWORKING OVER POWER LINE: WILL NEXT-GENERATION TECHNOLOGIES STUMBLE OR SHINE?

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EFFICIENT METHOD FOR INTERFACING TRIAC DIMMERS AND LEDs

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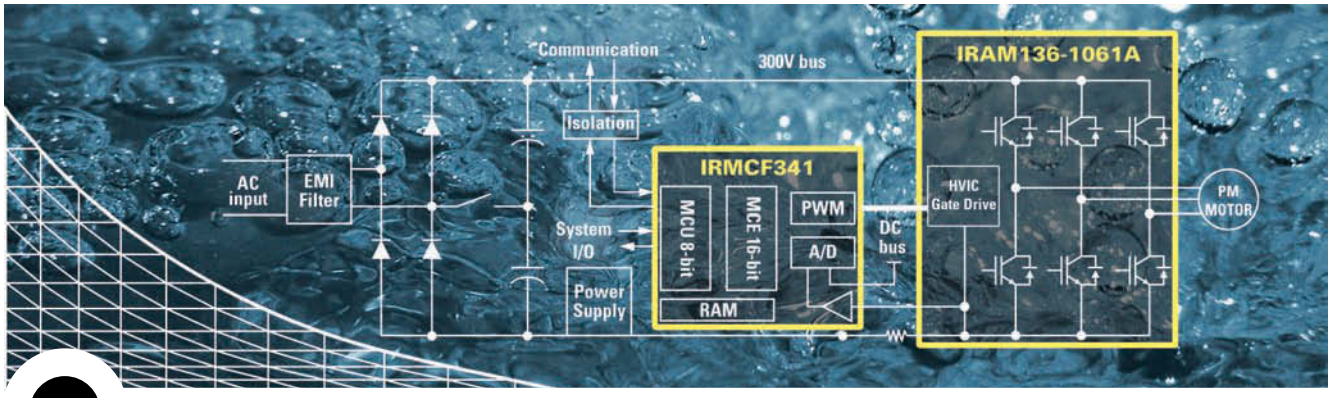

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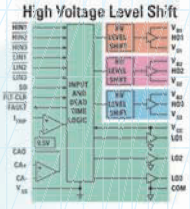

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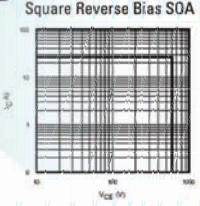

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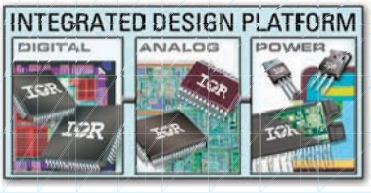

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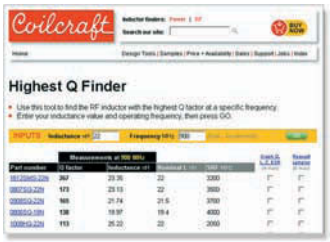

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Networking over power line: Will next-generation technologies stumble or shine?

by Brian Dipert, Senior Technical Editor

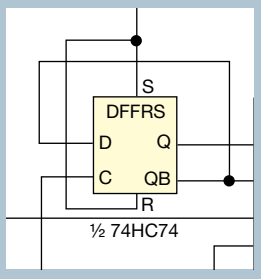
Efficient method for interfacing TRIAC dimmers and LEDs

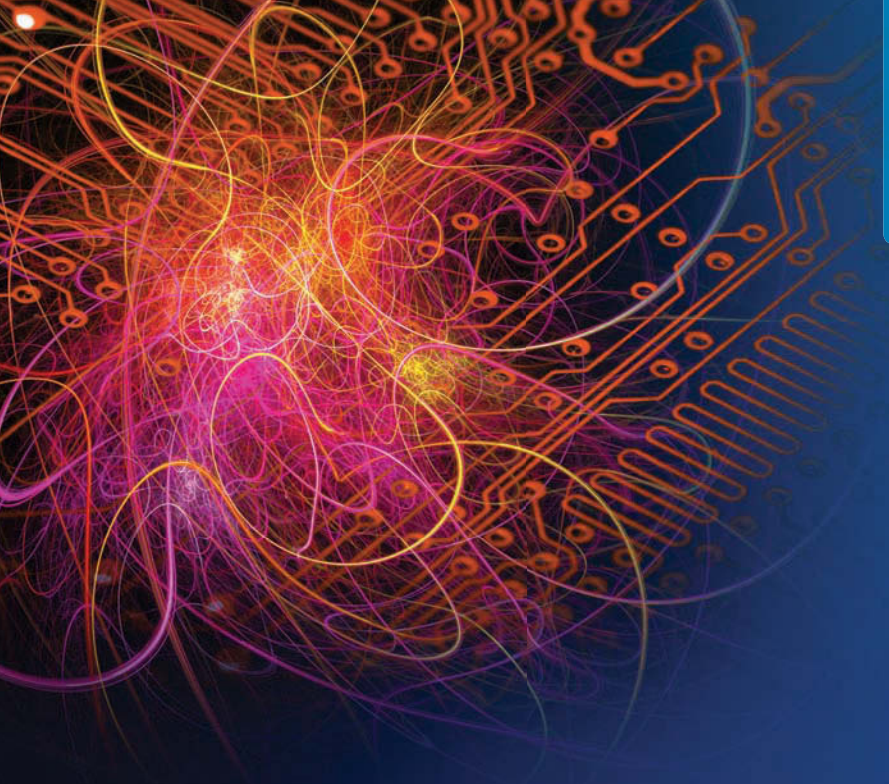
by James Patterson, National Semiconductor Corp

COVER: CJ BURTON

pulse

DESIGNIDEAS





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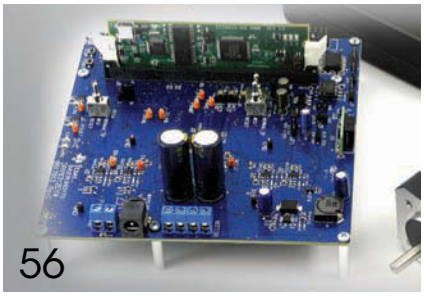

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FEATURED READER COMMENT

This issue's featured comment comes from an electrical engineer in response to the recent *EDN* design feature "Energy-efficient lights to gain from incandescent ban":

"The government should not be involved in mandating a change. As with all mandates, it does not take into account exceptions. For instance, there is no advantage to using a more expensive, less efficient bulb in places where it is not used much, like closets, refrigerators, and garages. There are other places where the radiant warmth of an incandescent bulb is welcome and useful, like in a bathroom. How will you use an LED bulb in an oven? And in the winter, the heat is not wasted."

EDN invites readers to constructively and creatively comment on our content. Share your comments at www.edn.com/110623tocd or visit www.edn.com/talkback.

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Volume 56, Number 12 (Printed in USA).

BY SUZANNE DEFFREE, MANAGING EDITOR, NEWS

Foxconn explosion ignites conversation on corporate responsibility

Combustible dust may have been to blame for an explosion that took place in May in a factory in Chengdu, China, killing three people and injuring 15. Apple-subcontractor Foxconn owns the factory, and the incident happened on a production line for Apple's iPad 2.

The short-term effect of this accident on the iPad supply may be minimal. It could mean that would-be iPad purchasers will have a longer wait for a new laptop. IHS iSuppli estimates that the incident could result in a production loss of 500,000 Apple iPad 2 tablets in the second quarter of this year, the equivalent of total iPad 2 monthly production capacity at the site. That estimate hinges on a return to full production pending the results of an investigation.

The long-term effect of the accident, however, will cause a much bigger flare-up. Reports claim that combustible dust gathered at the dust-collecting pipe in one of the polishing workshops. The US OSHA (Occupational Safety and Health Association) reported in 2006 that combustible-dust-related accidents have killed 119 and injured more than 700 people in the United States over the last 25 years.

An investigation may show that Foxconn's poor housekeeping caused the explosion. With three fatalities and so much public attention, however, China's government and others may crack down on factories that ignore the issue of combustible dust. New production regulations may come into force, affecting manufacturing in various ways, possibly seeing the shutdown of some electronics plants until they meet regulations.

The overarching question of corporate responsibility then comes into play. Is Apple—a US-based superpower company with huge worldwide name recognition and influence—responsible for workplace conditions at its partner companies? This question has come up repeatedly in the past, particularly when you consider that several Foxconn employees in 2010 committed suicide and blame was placed on workplace conditions. What precedent does it set if Apple takes corporate responsibility?

EDN's online audience has mixed reactions to these questions. Some adamantly believe that Foxconn and its local government, not Apple, should take full responsibility. For example, according to "Sparky Watt," posting on May 25, 2011, to make Apple responsible for working conditions at its suppliers would make all companies the "morals police." Demanding that Apple supervise other companies in this way is unfair to everyone, Watt writes, adding that the Chinese government and Foxconn—not Apple—are responsible for the explosion. Now that the issue has come out, Watt believes Apple should stop using Foxconn until the issue is resolved.

Other readers believe that Apple should shoulder some of the responsibility for work conditions at its partner companies. For example, reader "Elmer" wants to know how Apple could decline to take corporate responsibility for its product. "Just because the company hires offshore labor to build … products to improve margin does not mean that [Apple is] not responsible for its manufacture. [The company] dictates who builds products and how they build products. Who else is responsible? Foxconn is a subcontractor to Apple, which is the general contractor. If it were a building, the general contractor can't tell the client: 'It's not our fault; part of our team, which we chose and didn't tell you about, did it wrong,'" he writes.

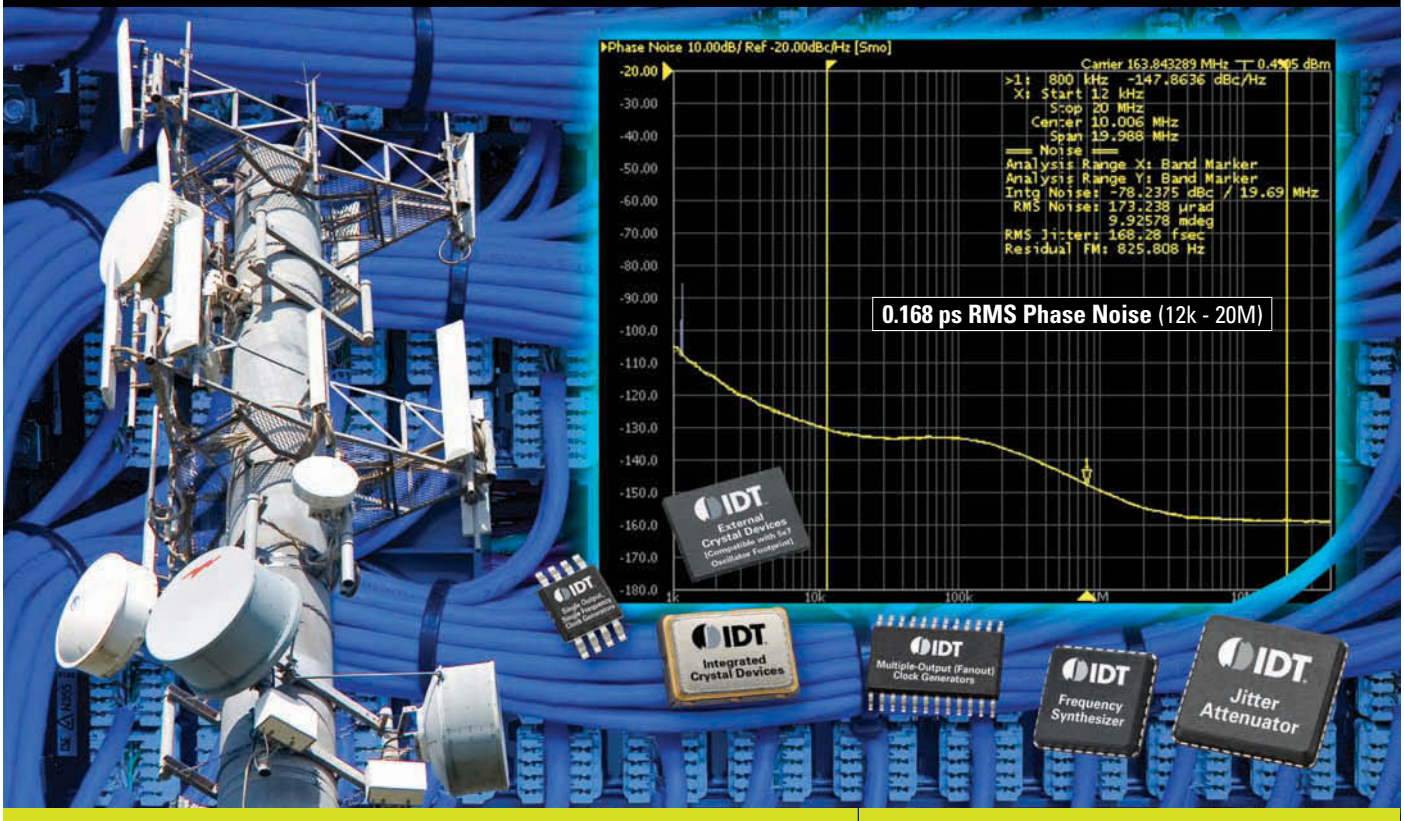
And still other readers place partial responsibility on consumers. A poster using the name "Reality" states that, "if Apple is responsible, then all [people] who purchase the item [manufactured at the plant] would in a way be responsible, too. Apple picked a questionable company. We picked Apple. No easy answer here. Up to a certain point, Apple should [ensure] workers' rights. But there is a limit."

Following on the heels of the Foxconn accident, another explosion took place at an Intel manufacturing plant in June in Chandler, AZ, injuring seven workers. Given these issues, more questions will certainly follow. This discussion is far from over.

What do you think? Join the conversation and share your thoughts at http://bit.ly/AppleFoxconn. EDN

Contact me at suzanne.deffree@ubm.com.

Integrated Device Technology FemtoClock NG – When a Trillionth Of a Second is Just Too Long



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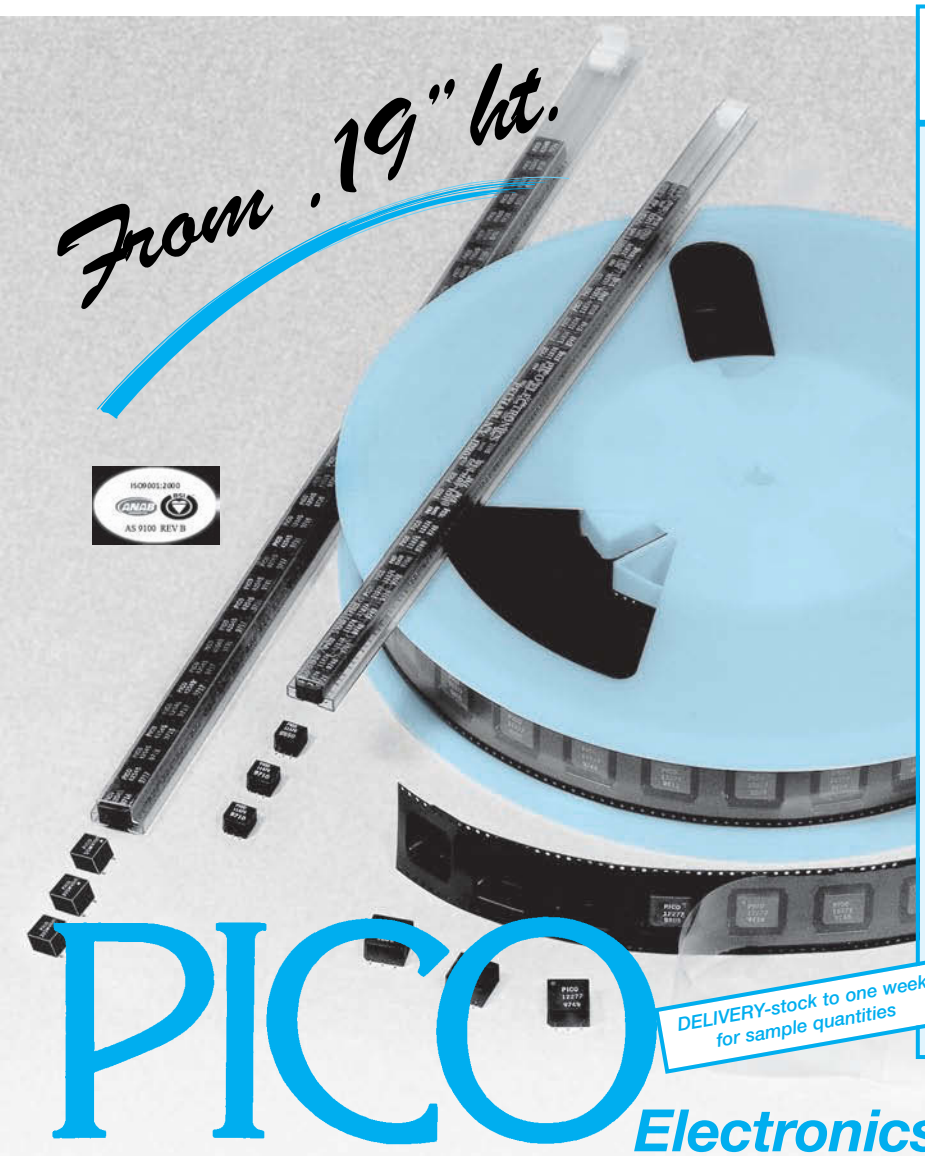

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INNOVATIONS & INNOVATORS

Single-board computer sports single- or dual-core Atom

WinSystems has announced the EPX-C380, an EPIC (Embedded Platform for Industrial Computing)-compatible, 1.66-GHz single-board computer. The 115×165-mm EPX-C380 uses Intel's single-core Atom N450 or dual-core D510 processor with an ICH8M I/O-hub controller, both of which are from Intel's Embedded Architecture Division to ensure long-term availability, which is desirable for embedded and industrial applications. Operating at –40 to +70°C, the unit provides an open platform for processor- and I/O-intensive medical, COTS (commercial-off-the-shelf)/military, security, transportation, pipeline, and machine-control applications.

The EPX-C380 uses the integrated Intel generation 3.5 graphics processor, which incorporates both VGA (video-graphics-adapter) and LVDS (low-voltage-differential-signaling) display interfaces with resolutions of 1400×1050 and 1366×768 pixels, respectively. Memory support includes as much as 2 Gbytes of DDR2 667-MHz SODIMM (small-outline-dual-inline-memory-module) system memory as well as a CompactFlash socket and an optional 2-Mbyte battery-backed SRAM.

The EPX-C380 has two GbE (gigabit-Ethernet) ports, two SATA (serial-advanced-technology-attachment) channels, and eight USB (Universal Serial Bus) 2.0 ports plus four RS-232/422/485 asynchronous serial channels onboard. A parallel port comprising 48 lines of digital I/O, high-definition audio, an LPT (line-printer) interface, a real-time clock, and a watchdog timer round out the onboard I/O. PC/104-Plus and MiniPCIe (Peripheral Component Interconnect Express) connectors enable expansion with either standard or user-designed specialty I/O modules.

The PC-compatible EPX-C380 architecture supports WES (Windows Embedded Standard) 7; Linux; Windows XP Embedded; and a vast software-development tool set, including device drivers and libraries. It also supports other x86-compatible real-time operating systems, such as QNX and VxWorks.

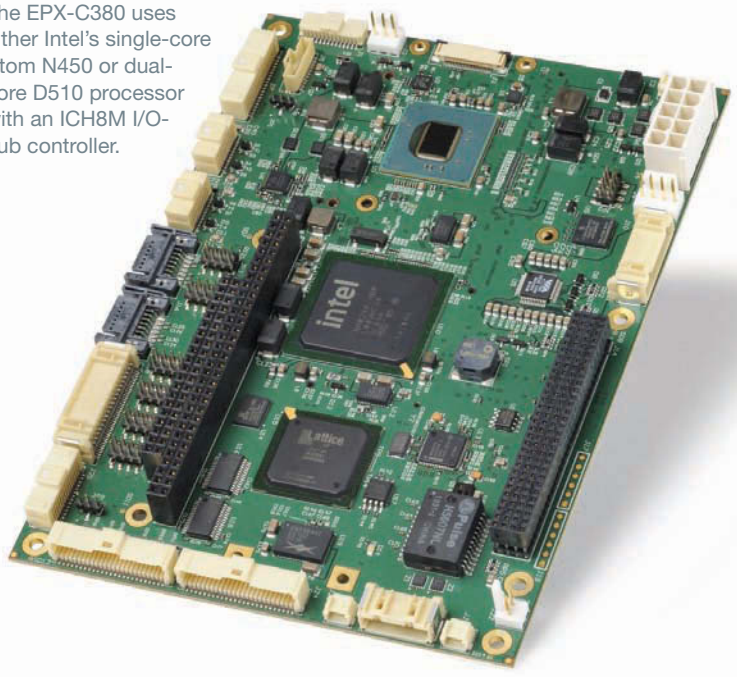
The EPX-C380 complies with ROHS (restriction-of-hazardous-substances) directives, requires only 5V, and typically draws 1.9A with 1 Gbyte of installed DDR SDRAM. The base price for a fanless, single-core N450-based board is $695. **—by Rick Nelson**

▷**WinSystems**, www.winsystems.com.

TALKBACK

"My biggest complaint with the engineering curriculum was that it did not adequately integrate theory with practice. … I'm pretty sure that a couple of my professors didn't know with certainty which end of the cord goes in the wall."

—EE Dave Alexander, in *EDN*'s Talkback section, at http://bit.ly/jaWfXK. Add your comments.



The EPX-C380 uses either Intel's single-core Atom N450 or dual-core D510 processor with an ICH8M I/O-hub controller.

Core-logic chip enhances predecessors' features

Intel's recently introduced Z68 Express Panther Point chip set enables motherboard and system designers to craft implementations that enable CPU and system memory overclocking, along with correspondingly raising the allowable current, voltage, and power-consumption thresholds. It also leverages the cost-effective on-CPU graphics core. And, even if you prefer to get your graphics fix over a PCIe (Peripheral Component Interconnect Express) bus or a few of them, you can still harness the LucidLogix (www.lucidlogix.com) Virtu software technology to tap into Intel's Sandy Bridge Quick Sync media-acceleration capabilities.

If the merging of H67 Express and P67 Express capabilities were all that Z68 Express offered, Panther Point would be just another chip set. Intel's got one more trick up its sleeve, however. Instead, Intel will augment its Rapid Storage technology drivers, which historically enabled features such as RAID (redundant-array-of-inexpensive-disks) 0/1/5/10 support, to enable an in-system solid-state drive to act as a high-performance front-end cache for a much larger hard-disk drive.

Smart Response technology, as Intel brands the technique, is conceptually old news. The company—to some extent in partnership with Microsoft (www.microsoft.com)—has for years been promoting the turbo-boost-memory concept; the Robson project targeted Windows Vista and leveraged the operating system's ReadyBoost technology. The Braidwood successor was more OS-agnostic and, taking advantage of falling semiconductor costs, beefed up the amount of flash memory devoted to the effort. A discrete turbo-memory subsystem offers some notable advantages over the hybrid-hard-drive alternative, which embeds a flash-memory cache within the rotating storage device. System OEMs aren't restricted to single-source specialized hard drives, for example, and they can also selectively include or exclude the flash-memory module in differentiating between cost- and performance-optimized system variants.

However, turbo-memory implementations have to date employed simplistic flash-memory single-component or multicomponent arrays mounted on MiniPCIe cards and the like, thereby necessitating system-CPU-based flash-memory-media-management algorithms that are OS-specific and therefore difficult to both develop and maintain. With Smart Response technology, Intel instead employs as much as 64 Gbytes' worth of conventional solid-state-drive capacity as caches. For larger drives, you can configure the remainder as a separate partition with a unique drive letter. Although managing data flow between the solid-state and hard-disk drives, conceptually comparable with RAID media-management routines, remains the responsibility of OS-specific high-level drivers, the onboard solid-state drive handles the low-level flash-memory-media-management algorithms.

Intel's new Z68 chip set adds features that its predecessors lacked.

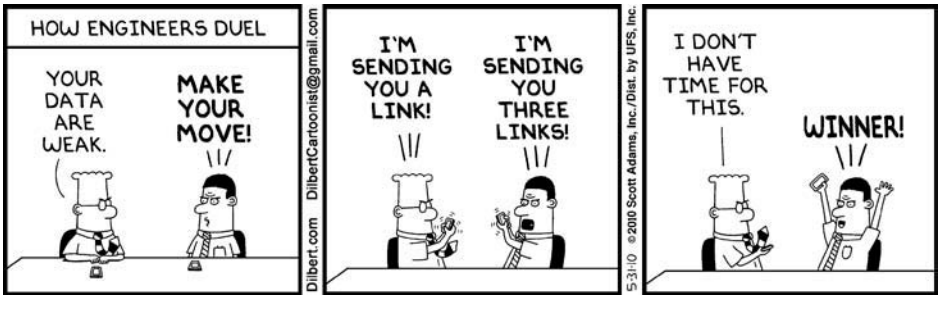
Intel only recently allowed the high-tech press to cover Panther Point; however, system partner Apple (www.apple.com) had been selling Z68 Express-based iMacs for more than a week before Intel welcomed the press. Apple offers Sandy Bridge iMac variants containing hard-disk drives, solid-state drives, and combos of both. Apple does not use Smart Response technology in the combination units. Doing so would present the hard-disk/solid-state-drive combo as one drive to the operating system. The company has, however, seemingly still enhanced the OS.

Mac OS X and its applications, along with any user's data-directory structure, have historically by default all resided on one drive or one RAID. Separating user data from its associated apps has been difficult to accomplish and left to users to negotiate. Apple's sales documentation now states that, if you configure your iMac with both the solid-state drive and a SATA (serial-advanced-technology-attachment) hard drive, it will come preformatted with Mac OS X and all your applications on the solid-state drive. You can use the hard drive for videos, photos, and other files.

The Z68 Express chip set costs $48 (1000). The company is also offering the Larsen Creek 311 series of solid-state drives, targeting Smart Response-technology applications and available in 2.5-in. SATA and mini-SATA form factors. The 34-nm, high-reliability, fast-writing, SLC (single-level-cell), flash-memory-based 311 series is a variant of the earlier-announced 310 mini-SATA and X25-M SATA product lines. The 20-Gbyte 311 series drives sell for $110 (1000). **—by Brian Dipert**

▷**Intel**, www.intel.com.

DILBERT By Scott Adams



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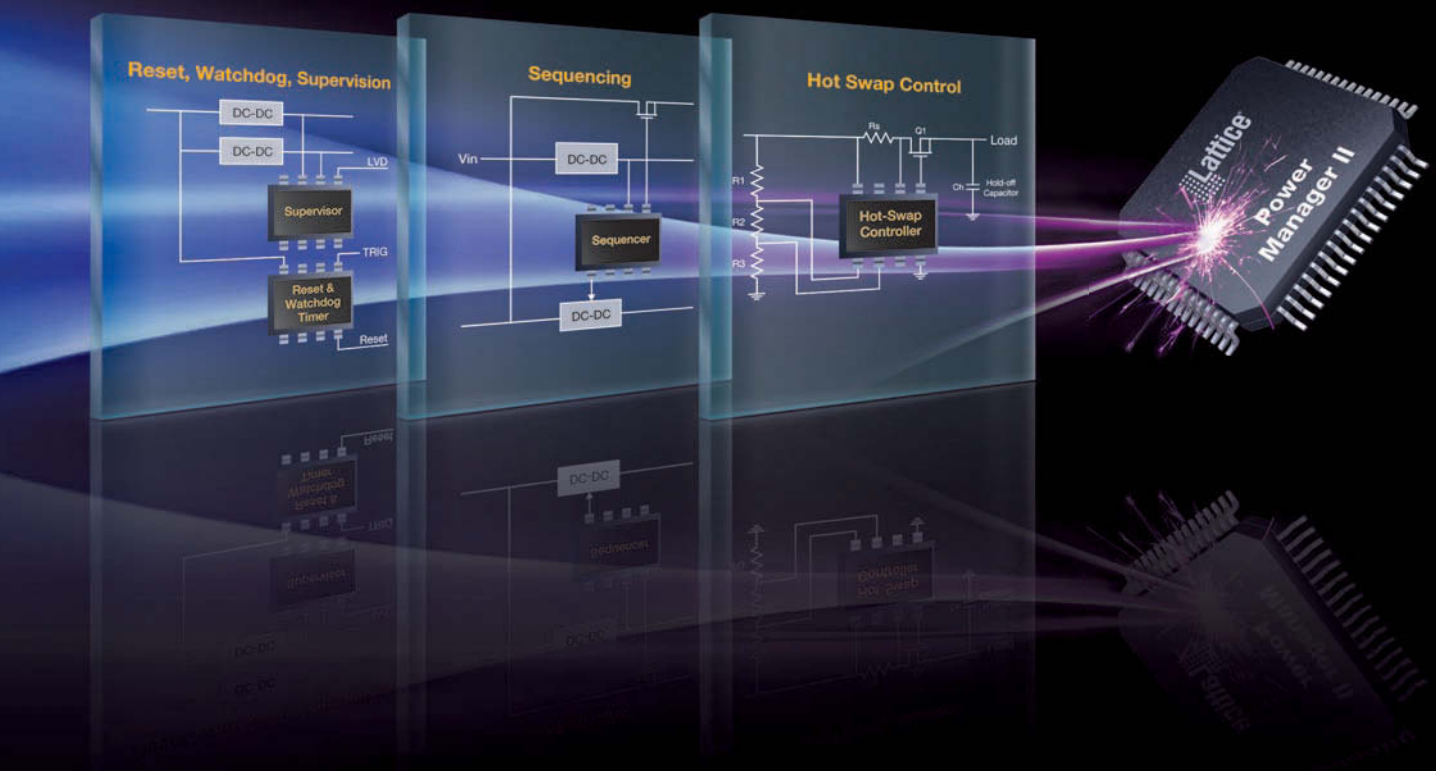

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Nanoscale pairings of particles show promise as miniaturized power sources

Scientists at the US DOE's (Department of Energy's) Brookhaven National Laboratory have assembled nanoscale pairings of particles that they believe show promise as miniaturized power sources. The researchers based their findings largely on quantum dots, nanometer-scale bits of semiconductor that are so small that electrical charges in the dots are confined in all directions.

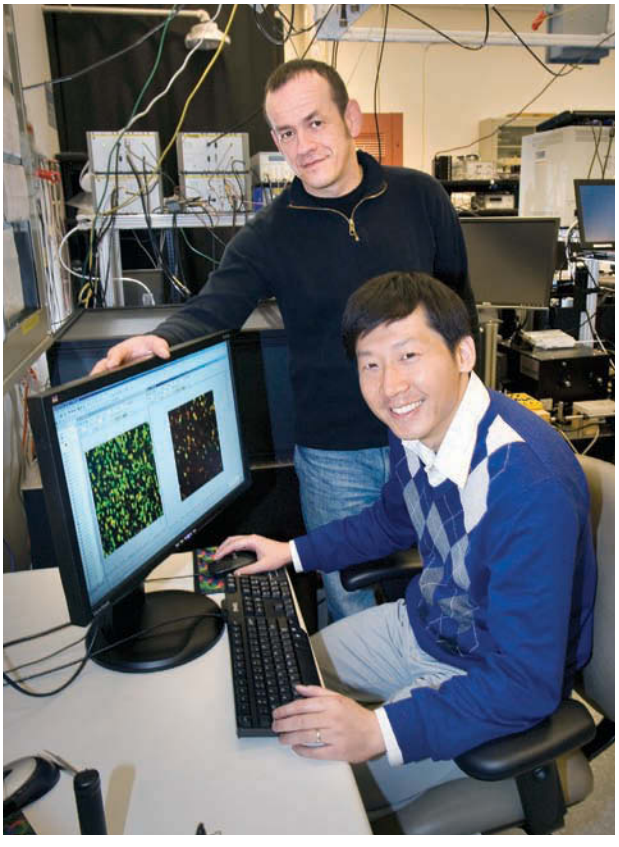
The lab's tiny dimeric, or two-particle, system comprises light-absorbing, colloidal quantum dots that link to carbon-based fullerene nanoparticles and convert light to electricity in a precisely controlled way. "This is the first demonstration of a hybrid inorganic/organic, dimeric material that acts as an electron donor-bridge-acceptor system for converting light to electrical current," says Brookhaven physical chemist Mircea Cotlet, lead researcher on the experiments on dimers and their assembly method.

By varying the length of the linker molecules and the size of the quantum dots, the scientists can control the rate and the magnitude of fluctuations in light-induced electron transfer at the level of the individual dimer. "This control makes these dimers promising power-generating units for molecular electronics or more efficient photovoltaic solar cells," says Cotlet, who conducted this research with materials scientist Zhihua Xu at Brookhaven's CFN (Center for Functional Nanomaterials).

Researchers have recently combined quantum dots with electron-accepting materials, such as dyes, fullerenes, and titanium oxide, to produce dye-sensitized and hybrid solar cells in the hope that the light-absorbing and size-dependent emission properties of quantum dots would boost the efficiency of such devices. The power-conversion rates of these systems have remained low.

"Efforts to understand the processes involved … to engineer improved systems have generally looked at averaged behavior in blended or layer-by-layer structures rather than the response of individual, well-controlled hybrid donor-acceptor architectures," says Xu. The assembly process takes place on a surface and in a stepwise fashion to limit the interactions of the particles, which could otherwise combine in a number of ways if the researchers used solutions for assembly. This surface-based assembly also achieves controlled, one-to-one nanoparticle pairing, the scientists claim.

The scientists vary the size of the quantum dots, which absorb and emit light at different frequencies according to their size. They also vary the length of the bridge molecules connecting the nanoparticles. For each arrangement, they measure the electron-transfer rate using molecule spectroscopy. These efforts help to identify the optimal architectural arrangement for the particles. "This method removes ensemble averaging and reveals a system's heterogeneity—for example, fluctuating electron-transfer rates—which is something that conventional spectroscopic methods cannot always do," Cotlet explains.



Physical chemist Mircea Cotlet (standing) and materials scientist Zhihua Xu are leading an experiment on pairing quantum dots with fullerenes for nanoscale photovoltaics (courtesy Brookhaven National Laboratory).

> Surface-based assembly achieves controlled, one-to-one nanoparticle pairing.

The scientists found that reducing quantum-dot size and linker-molecule length led to enhancements in the electron-transfer rate and suppression of electron-transfer fluctuations. "This suppression of electron-transfer fluctuation in dimers with smaller quantum-dot size leads to a stable charge-generation rate, which can have a positive impact on the application of these dimers in molecular electronics, including potentially in miniature and large-area photovoltaics," Cotlet says.

"Studying the charge separation and recombination processes in these simplified and well-controlled dimer structures helps us to understand the more complicated photon-to-electron-conversion processes in large-area solar cells and eventually improves their photovoltaic efficiency," says Xu.

A US patent application is pending on the method and the materials resulting from using the technique. The technology is available for licensing. The DOE's Office of Science funded the researchers' work.

—by Suzanne Deffree

▷**Brookhaven National Laboratory**, www.bnl.gov.

RAQ's

Rarely Asked Questions

Strange stories from the call logs of Analog Devices

Do Something with that Unused Pin!

Q: What should I do with the unused terminals of analog ICs?

A: Treat them with kindness and consideration—never ignore them.

According to Goethe, "An unused life is an early death."[1] Similarly, an unused pin on an analog IC may greatly increase the risk of its early death by electrostatic discharge (ESD). Although unused outputs may, and generally should, be left unconnected, it is usually best to connect unused inputs, both analog and digital, to a supply. The connection will usually be to the negative ground in a single-supply system and to the center rail in a dual-supply system—but there are important exceptions. As always, it is essential to RTFDS (Read The Friendly Data Sheet[2]) and do as it advises. If there is no mention of the topic, however, grounding is usually the best policy.

Unused amplifier inputs are one of the important exceptions. As we saw in RAQ Issue 46[3], grounding an unused amplifier's inputs may increase its current consumption, so the best policy here, and often the only safe one, is to connect the amplifier as a buffer, tying the input to a potential somewhere between the supply rails.

CMOS switches and multiplexers are symmetrical devices; their signal input and output terminals are interchangeable, so unused ones should all be considered to be inputs, not outputs. Thus, they should all be grounded. The reasons for this were discussed in more detail in RAQ Issue 3.[4]

Internal pull-up or pull-down resistors connect an input to a positive supply (pull-up) or ground (pull-down). If an unused input

has one of these resistors, it is not necessary to make any connection to it. If the pin is tied down, however, it should be connected to the same supply as its resistor, as any other connection will cause current to flow in the resistor, wasting power (the wasted power is likely to be quite small, but any waste is to be avoided if possible).

It is particularly important to consider unused logic inputs, as some must be tied to Logic-1 when unused. Also some logic inputs have three states, not two, with the open circuit condition defined as a logic state. Such inputs may need to be left unconnected.

To summarize, considering the connection of unused IC pins is an important part of the analog circuit design process and must never be overlooked.

[1] Johann Wolfgang von Goethe - from his play "Iphigenie in Tauris" (1779).
[2] RAQ Issue 4 – "Caveat Emptor."
[3] RAQ Issue 46 – "What shall we do with the Unused Op-Amp?"
[4] RAQ Issue 3 – "Isolating the Key Detail (or Lunching With a Mermaid and Pickled Herring)."

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Contributing Writer James Bryant has been a European Applications Manager with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur. Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

Have a question involving a perplexing or unusual analog problem? Submit your question to: www.analog.com/askjames

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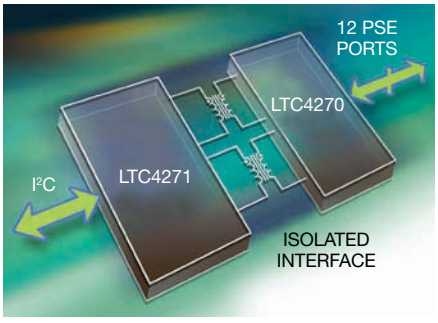
Chip set pushes 12-port POE PSE to 90W per channel

The original version of the POE (power-over-Ethernet) standard specifies 13W for each powered device; the latest version, IEEE 802.3at, POE+, increases the power to 25.5W. However, POE-powered devices' increasing number of features and new industrial applications are driving the need for ever-increasing amounts of power. For example, power adapters for laptops require 60 to 90W, and POE applications on the factory floor can require higher power to drive actuators and controls.

To address these changing needs, Linear Technology has developed the LTPOE++ version of POE, which can power as much as 90W per port. A version of the company's LTC4270/LTC4271 chip set for PSE (power-sourcing equipment) uses LTPOE++ to deliver as much as 90W of power to as many as 12 LTPOE++-powered devices. LTPOE++ uses proprietary signaling methods to identify LTPOE++-powered devices requiring more than the 25.5W limit of the POE+ specification. LTPOE++ is interoperable and backward-compatible with IEEE POE/POE+-compliant devices, so LTPOE++, POE+, and POE devices can seamlessly work together.

The LTC4271 provides a digital interface to the PSE host, and the LTC4270 acts as a high-voltage Ethernet interface, delivering power to the 12 independent POE ports. Two low-cost Ethernet transformers bridge the two ICs, providing galvanic isolation, replacing as many as six optocouplers, and eliminating the need for an isolated 3.3V supply.



The LTC4270/LTC4271 chip set for POE power-sourcing equipment uses the proprietary LTPOE++ to deliver as much as 90W of power to as many as 12 LTPOE++-powered devices.

The LTC4270 is available in three power grades. The A Grade uses Linear's LTPOE++ signaling to support powered devices requiring as much as 90W of power. The B Grade uses POE+ signaling to support devices requiring as much as 25.5W, and the C Grade uses POE signaling to support devices requiring as much as 13W. The LTC4270 comes in an ROHS (restriction-of-hazardous-substances)-compliant, 52-pin, 7×8-mm QFN package, and the LTC4271 comes in a 24-pin, 4×4-mm QFN package. Prices for the LTC4270/LTC4271 chip set start at $12 (1000).

—by Margery Conner

▷**Linear Technology Corp**, www.linear.com.

06.23.11

Language-based environment targets embedded-system verification

Kozio, a provider of in-system diagnostics, has announced ValidationAssistant, a unified, interactive, embedded-hardware-verification environment that simplifies hardware control, automates test execution, and maintains test cases in a structure that facilitates reuse across an entire product life cycle, including engineering, production, and field test. The PC-based application interacts with any DUT (device under test), executing Kozio's kDiagnostics bare-metal in-system diagnostics software without requiring an operating system. The ValidationAssistant and kDiagnostics environment forms a suite of software tools for board diagnostics, binary-image downloading, in-system programming, automated board testing, and power-on self-test. Features include high-level commands for each design and a point-and-click interface that together accelerate the control and execution of functional board-level tests. Using one command, you can test an entire board within minutes at the hardware's full operating speed.

Vince Mazur, market-development director at Kozio, explains that host-resident ValidationAssistant interacts with the company's target-resident kDiagnostics tool to automatically validate hardware designs, support the optimization of embedded-system performance, and simplify the integration of new software and hardware. The tool replaces previous methods involving terminal emulators that interface target and host, which can require that firmware engineers write the embedded code for menu and prompt creation and modify that code for each new design. ValidationAssistant provides a language-based environment for the development of repeatable, point-and-click-initiated, embedded-system-level tests in hardware, free from operating-system and other higher-level software abstractions.

The combination of ValidationAssistant and kDiagnostics lets users observe and control behavior at the hardware boundary, transforming ad hoc approaches into ordered, repeatable methodologies. Users can program EEPROM, NAND, NOR, and FPGA devices and CPLD (complex programmable-logic devices); read and write memory; peek and poke hardware registers; control interfaces; access and configure connected devices; configure power settings; and maximize IP (intellectual-property) reuse. The tools form a reusable approach that promotes collaboration among engineering teams, contract manufacturers, and ecosystem partners—from design verification and characterization through production test, in-field diagnostics, and returns testing.—by Rick Nelson

▶**Kozio, www.kozio.com.**

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Open-source hardware suits kitchen-table start-up

Last month, I attended Maker Faire (www.makerfaire.com) in San Mateo, CA. According to its Web site, the fair is the "premier event for grassroots American innovation … and the world's largest do-it-yourself festival." While I was there, the Seeed Studio (www.seeedstudio.com) booth caught my eye. I was familiar with Seeed, whose founder, Eric Pan, noticed an untapped need in the United States from engineers who have good ideas but lack the know-how and capital to start a production line. In response, Seeed has diversified into offering not only production capabilities but also stocking, order fulfillment, and basic marketing for electronic products that independent engineers design. Seeed Studio's first partner is Ian Lesnet. Lesnet's protocol debugger, Bus Pirate, became the first product of his new company, Dangerous Prototypes (www.dangerousprototypes.com). In just two years, the company has grown to include more than 15 products and eight employees. I recently had a discussion with Lesnet, a portion of which follows.

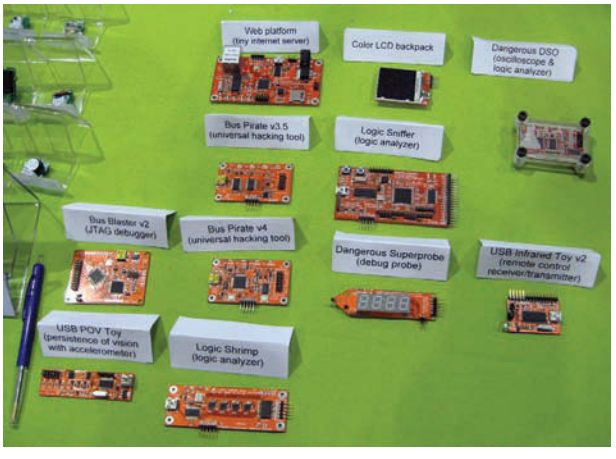
OSS [open-source software] is a familiar concept, but what is OSH [open-source hardware]?

A OSS [describes a scenario in which] you release source code and allow people to reuse it. OSH isn't much different: You release the design files for the PCBs [printed-circuit boards] as well as the code that runs on the circuit's microcontroller—if it has one. With OSH, you're giving people permission to use your design.

What's the appeal of OSH to a hardware start-up? Is there a problem with losing your IP [intellectual property]—your design? Why would you want to expose that IP?

A We take as much as we give. We build on work that others have done, and it gives us a jump-start on our design. For example, for Dangerous Prototypes' [new] logic analyzer, someone has put hundreds of hours of work into its code. All I did was design a PCB for it. The original code was written for a generic development platform. We wondered about the cheapest piece of hardware that could run this code. We ended up using a PIC microcontroller and Xilinx FPGAs and PLDs. They're programmed with software that's available for free—not necessarily open source, but free—so anyone can compile our source code. There's no barrier for anyone else to do it.

If someone wants to take the time, energy, and money to make my things and sell them and, in doing so, publicize my company, why should I stop them? Even if we wanted to, we're too small. I'm not going to hire a lawyer to go after someone; I don't even have the time to write a nasty letter.



Dangerous Prototypes has created and sold 15 products since it started two years ago.

How did you and Seeed Studio find each other?

A For fun, I wrote some protocol-debugging code that I posted on my blog while I was employed full-time elsewhere. Pan knows how frustrating it can be to debug communication protocols, so, when he found the blog post online, he suggested that I design hardware that would work in tandem with the software to make a more powerful debugging tool. I had several ideas for what types of hardware would assist in debugging and hacking hardware but hadn't considered producing a product because of my lack of production and marketing experience. Seeed Studio had access to both.

Your Web site says it releases a new open-source project every month. What's that about?

A Our goal is to make the hardware available from Seeed the day we publish the design. When we started, we were a shoestring operation, [and I worked] on my kitchen table by myself. We would do presales; people would order the project ahead of time; when we reached a critical mass of orders, we would go ahead with the manufacturing. [Seeed Studio requires a minimum order of 100 pieces.]

How do you handle customer support?

A We have a forum and encourage people to post within the forum. I try to answer all questions within an hour, but we have such a great community that someone will usually jump in and answer a question if I don't get to it right away. I couldn't do it without the community.

Do you think there's a future in this approach for other US engineers?

A Yes! It's worked great for Dangerous Prototypes.

—interview conducted and edited by Margery Conner

"How can I tell if a power supply is reliable?"

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BY BONNIE BAKER

Signal integrity and characteristic impedance

Signal-integrity problems can present some interesting issues as you try to stabilize the signals across your board. The IBIS (input/output-buffer-information-specification) model provides a simple approach to these problems. You can use an IBIS model to extract important variables for your signal-integrity calculations and PCB (printed-circuit-board) designs. The values that you extract from the IBIS model are integral parts of the signal-integrity-design calculations.

As you tackle transmission-line-matching issues in your system, you must understand the electrical impedances and characteristics of your ICs and PCB traces. **Figure 1** shows a single-ended transmission line. With your transmission line, you can extract the transmitter's output impedance, Z_T, and the receiver's input impedance, Z_R, from the IC's IBIS model. These IC specifications are sometimes unavailable in the IC manufacturer's product data sheets, but you can pull all of these values from the IBIS model.

Four parameters define transmission lines: characteristic impedance, Z_0; board propagation delay, D; line propagation delay t_D; and trace length. Typically, the FR (flame-retardant)-4 board's characteristic impedance ranges from 50 to 75Ω, and propagation delay ranges from 140 to 180 psec/in. The characteristic-impedance values depend on the actual transmission line's material and physical dimensions (**Reference 1**). The line delay on your board equals the propagation delay times the length of your trace. With any board, $D=10^{12}\sqrt{(C_{TR}\times L_{TR})}$, or D=85 psec/in.$\times\sqrt{(e_R)}$; $Z_0=\sqrt{L_{TR}/C_{TR}}$; and t_D=D×LENGTH, where C_{TR} is the trace capacitance, L_{TR} is the trace inductance, and e_R is the PCB-material dielectric constant. For FR-4 boards, a reasonable strip-line propagation delay is 178 psec/in., with a characteristic impedance of 50Ω.

The transmitter specifications for a signal-integrity evaluation are output impedance, Z_T. When determining the output impedance, the pin area in the IBIS model provides each pin's resistive, inductive, and capacitive parasitic values. You then join the package capacitance with the respective buffer's capacitive value, C_comp, to get a better picture.

A pin keyword relates to a package, as the component, manufacturer, and package above the pin keyword describe. You will find the package capacitance and inductance in the pin's keyword table as it relates to the pin of interest. For instance, in the ads129x.ibs model (**Reference 2**), **Listing 1**, available with the Web version of this article at www.edn.com/110623bonnie, shows where you would look for the L_pin and C_pin values of signal GPIO4, pin 5E (64-pin PBGA package). The pin inductance and pin capacitance for this signal and package are 2.5339 nH and 0.28001 pF, respectively.

The second capacitance value of interest is the C_comp value under the model keyword. As you find the correct model in the IBIS model, you will find a list of C_comp values. **Listing 2**, available at www.edn.com/110623bonnie, shows an example of C_comp in the DIO_33 model (**Reference 2**).

In the statements in **Listing 2**, the | symbol indicates a comment. The text highlighted in yellow shows the active C_comp (**Reference 3**). From these lines in the **listing**, the PCB designer can choose among three values. During the PCB transmission-line design stage, the typical value of 3.072722 pF is an appropriate choice.

The IBIS model provides clues for PCB designers who perform board simulations before moving to the prototype stage. If you know where to look, the IBIS model provides the characteristic impedance and capacitance of all the pins. The next step in this evaluation is to determine the I/O resistance of each buffer. You will see this topic in a future column. EDN

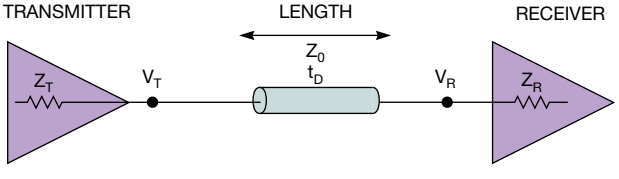

Figure 1 With your transmission line, you can extract the IC transmitter's output impedance, Z_T, and receiver's input impedance, Z_R, from the IC's IBIS model.

REFERENCES

1 Johnson, Howard, and Martin Graham, *High-Speed Digital Design: A Handbook of Black Magic*, Prentice Hall, 1993, ISBN: 9780133957242.
2 ads129x.ibs, IBIS Model, sbam021b, Texas Instruments, http://bit.ly/mJ7FNH.
3 Baker, Bonnie, "Beyond the data sheet with IBIS," *EDN*, May 26, 2011, pg 22, http://bit.ly/kQI7No.

Bonnie Baker is a senior applications engineer at Texas Instruments.

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Bulldog Security RS82B remote-vehicle-starter system

A diligent press-relations person offered me a remote-starter system to evaluate. I explained that, because *EDN* is a highly technical magazine, my evaluation would require that I take the starter apart. The company was OK with that. I was able to pry into the guts of the microprocessor-controlled unit as well as the RF key fob you use to operate it. I was astonished to see that the remote operated from 12V. The main unit provides an excitation coil for your car's spare smart key so that the unit can disable the car's security system when you start it remotely. The 400-foot range sounds nice, but this unit works only on automatic-transmission cars built after 1996, so my '92 Honda can't use it.

This large copper winding excites a spare car key that you clamp in the foam holder. It allows the system to excite the key and turn off your car alarm.

Two large and five small relays interface with the car's starting circuits. You can't beat a relay for isolation or low on-resistance, as well as low cost. The relay manufacturer is a Chinese company, Sanyou, not Sanyo of Japan.

Parts reside on both sides of the PCB (printed-circuit board). They include a Texas Instruments relay driver and National Semiconductor op amps.

An 8-bit 46R0662 Holtek microprocessor with ADCs, in a 44-pin QFP, controls the system.

A double-sided PCB has parts on one side only. A 20-bit Zhengxin Microelectronics LX-2240B remote-control-encoder IC holds 1 million codes. You apply the 12V battery to the chip when you press either button. The RF amplifier is an NPN transistor with a crystal tank circuit.

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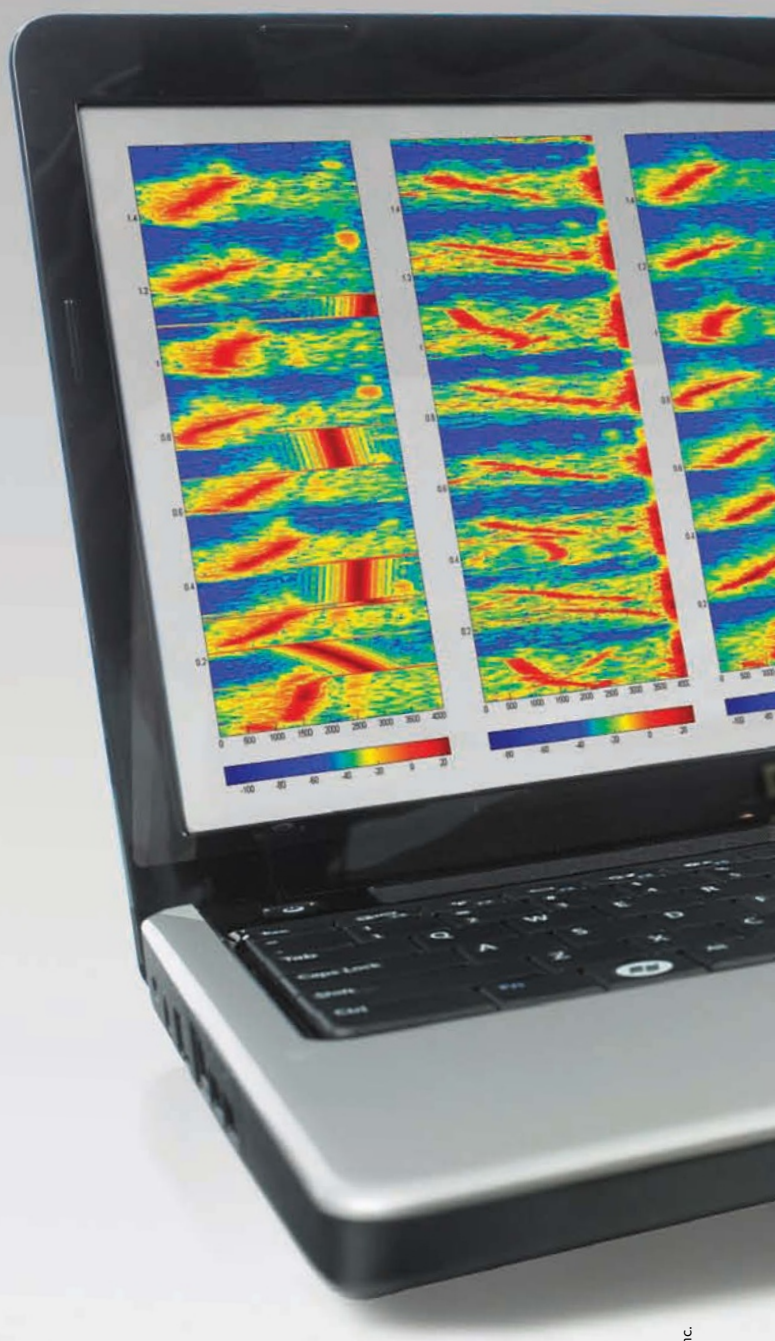

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MECHATRONICS IN DESIGN

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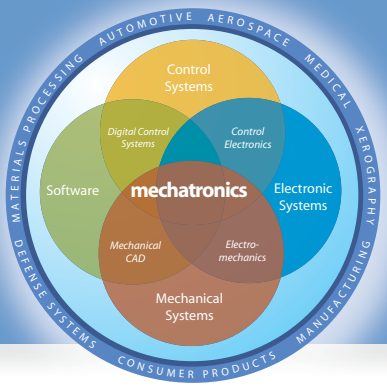


Modeling and simulation for motor selection

Trajectory planning, system modeling, and control design are essential for motor selection.

Multidisciplinary engineering systems are complex and carry increased risk, development time, and integration challenges. Model-based system design helps to manage complexity, enhance integration, and reduce the development time and risk. How does model-based design improve motor selection for a motion application, however?

First, consider that system requirements dictate a desired endpoint trajectory (**Figure 1**). You can define the motion as an electronic cam. Different profiles and maximum values of velocity, acceleration, and jerk define this cam, and these profiles affect the level of mechanical stress, vibration, and noise in the motor, transmission system, and mechanical load. It is therefore essential that you first choose a motion profile because the required torque-versus-speed curve to size the motor depends on it. The profile also affects the tracking errors through the control system.

You then develop a geometry-of-motion, or kinematic, model of the mechanical system and determine the required motion profile through inverse kinematics. The torque-speed requirements for the motor are determined by first developing a kinetic model of the complete mechanical system. This model encompasses geometry plus all torques and mass moments of inertia. You then apply an appropriate feedback-control system, such as a PID (proportional-integral-derivative) system, to that model. Using MathWorks' (www.mathworks.com) Matlab or Simulink, you can derive a computer simulation of the mechanical and control systems, which will provide you with the necessary torque-speed curve of the load to size the motor.

Kevin C Craig, PhD, is the Robert C Greenheck chairman of engineering design and a professor of mechanical engineering at Marquette University's College of Engineering. For more mechatronics news, visit mechatronicszone.com.

Once this process is complete, you can identify candidate servo motors, such as permanent-magnet synchronous motors. Considering cost, energy efficiency, and load-to-motor inertia ratio shortens the list. The chosen motor and its properties must be included in the system model. The control system will have to be tuned or even modified because of the motor addition.

A computer simulation reveals new torque-speed requirements for the system by presenting a number of issues. For example, it determines whether the motor's torque speed is satisfactory; the control system is stable; and the system meets application-specific requirements regarding time response, relative stability, and steady-state error. If the system fails to meet any of these criteria, you must rerun your simulation. Once you thoroughly analyze these factors, you will find that a model-based design and computer simulation can ease motor selection and optimize overall system performance. EDN

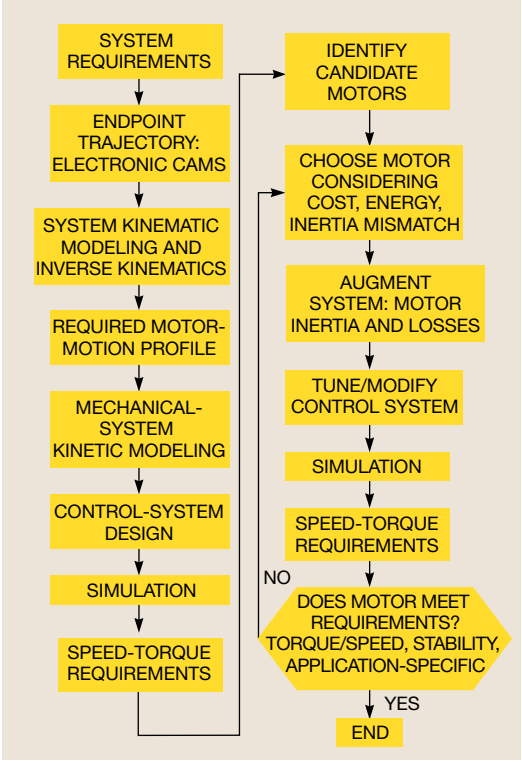
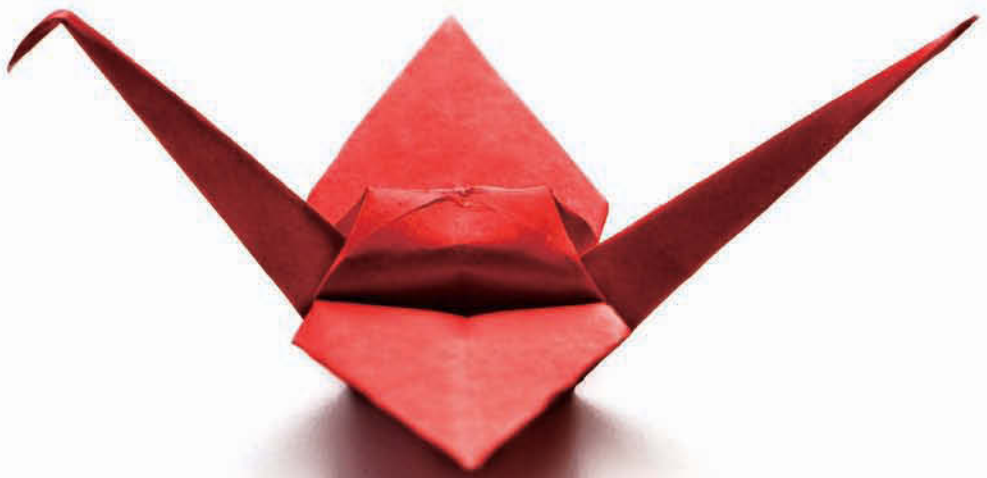


Figure 1 System requirements dictate a desired endpoint trajectory.

ARIGATO

- Thank you -



As your trusted partner

We would like to extend our heartfelt gratitude for your concern, assistance and cooperation to us during the difficult time after the earthquake. Our entire staff is currently working hard to achieve an early recovery.

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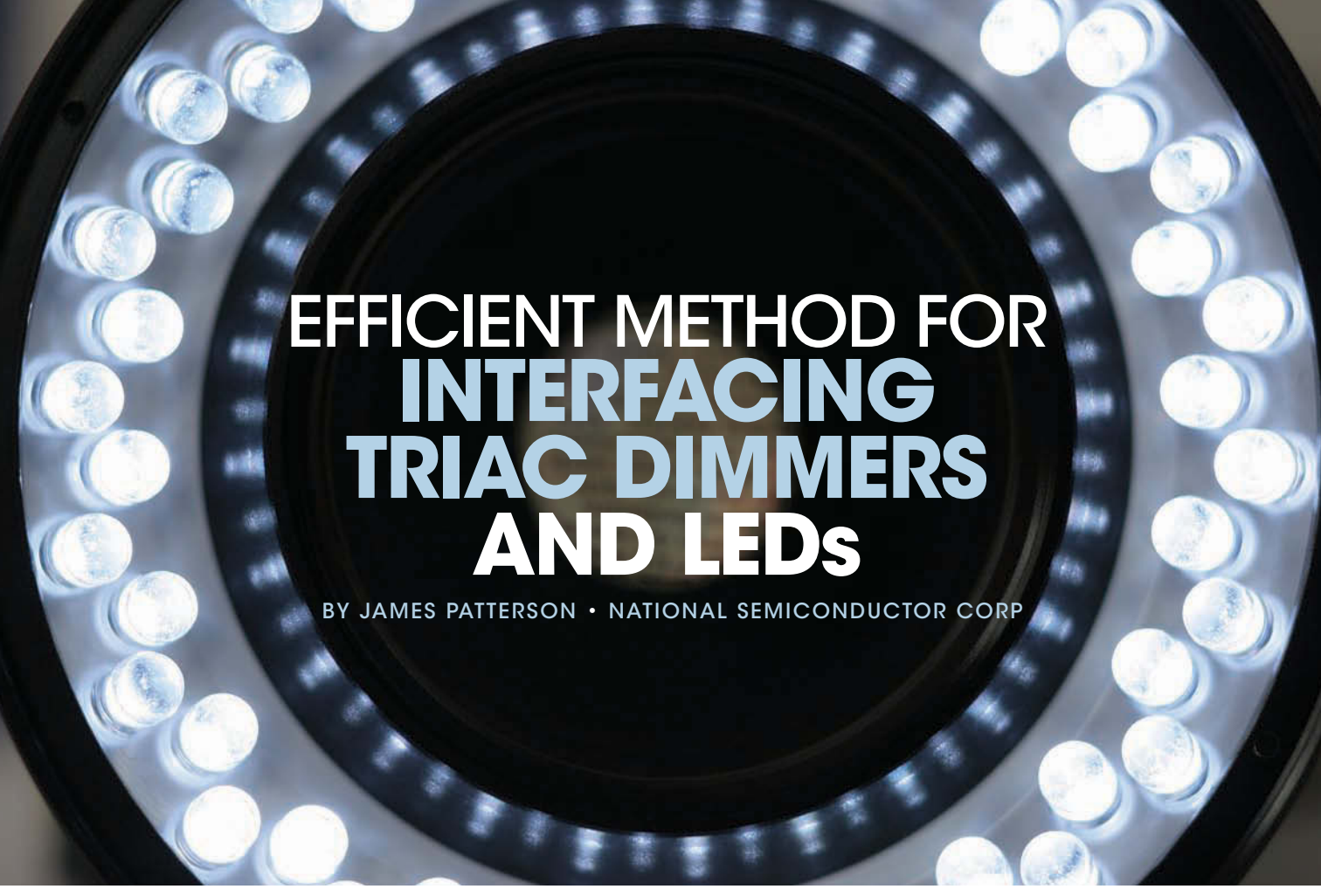

EFFICIENT METHOD FOR INTERFACING TRIAC DIMMERS AND LEDs

BY JAMES PATTERSON • NATIONAL SEMICONDUCTOR CORP

THERE ARE MORE THAN 2 MILLION INSTALLED TRIAC DIMMERS WORLDWIDE, AND THEY CAN PROVE A CHALLENGE TO THE CONTROL CIRCUITRY OF AN LED LIGHT. WITH SUCH A LARGE BASE, BACKWARD COMPATIBILITY IS A MUST.

The lighting industry has relied on the incandescent bulb for more than a century, and, over the last 50 years, the phase dimmer has become the main dimming control. Standard forward-phase, or TRIAC (triode-alternating-current), dimmers are notoriously difficult to interface with LED drivers. To make things worse, the performance of each dimmer varies greatly. Although there are newer, better reverse-phase dimmers available, the standard forward-phase dimmer is so common in the world's electrical infrastructure that LED-lighting manufacturers simply cannot ignore it. As usual, backward compatibility is paramount.

FORWARD-PHASE DIMMERS

A standard forward-phase dimmer contains a TRIAC, a DIAC (diode-alternating-current), and an RC (resistance/capacitance) circuit (**Figure 1**). A potentiometer controls the resistance, and the resulting RC time constant controls the amount of delay before the TRIAC turns on, or the firing angle. The portion of time when the TRIAC is on is the conduction angle, θ. The resulting voltage waveform is a phase-cut sinusoid.

This type of dimming works well in incandescent bulbs, which are simple resistive loads. The time-averaged voltage across the filament's resistance decreases as the conduction angle decreases, providing naturally smooth dimming.

The TRIAC also has a minimum holding-current requirement. The cur-

IMAGE: THINKSTOCK

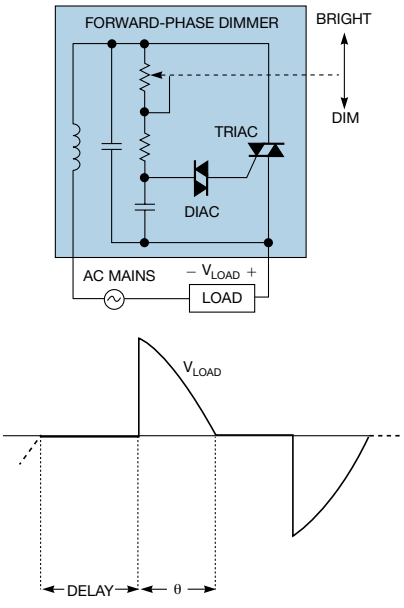

Figure 1 A standard forward-phase dimmer contains a TRIAC, a DIAC, and an RC circuit.

rent flowing through the TRIAC must remain above this minimum level to ensure that it remains on throughout the entire conduction angle. The incandescent load easily satisfies this condition because of the load's inherent power levels—40, 60, and 75W, for example.

COMPATIBILITY WITH LEDs

Unfortunately, solid-state lighting lacks the benefits of the phase-dimming approach. An LED is a semiconductor device; controlling light output is accomplished by regulating its forward current. High-brightness LEDs, which can conduct hundreds of milliamps to amps of current, almost always use a switching converter to maintain system efficiency.

A standard switching converter regulates its output regardless of the average input voltage, meaning that the phase-chopped waveform that the phase dimmer provides must first be decoded. The decoded information can be used to control the reference for output regulation. Although this task is relatively simple for power-electronics designers, many complexities hide under the surface.

AT A GLANCE

- LED lights must be backward-compatible with the installed base of 2 million TRIAC (triode-alternating-current) dimmers.
- Maintaining compatibility requires some loss of efficiency by the LED light.
- Future dimming approaches may provide dimming with no additional inefficiency in the LED lights.

An obvious difference is that the load is no longer purely resistive. Instead, the converter looks like a reactive load to the phase dimmer due to both capacitive and inductive components within the circuit. This condition causes a standard converter to have problems with the fast rising edge of the phase-chopped voltage. Designers usually will employ standard RC-damping methods to reduce the problematic ringing that this rising edge induces. However, this approach always involves extra power loss.

An even larger problem comes from an unexpected source. The efficacy of modern LEDs is far superior to that of incandescent bulbs, which waste more than 75% of their light output in the infrared spectrum as heat. LEDs, on the other hand, provide most of their light output in the visible spectrum. The newest high-brightness LEDs are five to six times more efficient than comparable incandescent lights, meaning that a current LED replacement for a 60W bulb or fixture could be as low as 10 to 12W. This power savings is great for the consumer but not for the phase dimmer, which has the minimum holding-current requirement.

When dimming an LED fixture, the TRIAC may misfire—that is, conduct insufficient current to remain on for the whole conduction angle. Because the misfires are usually asymmetrical in consecutive rectified ac-line cycles, the decoded angle can oscillate between two or more points. This oscillation manifests itself as visible flutter and flicker of the light output because of the low frequency. To prevent visible flicker, the converter must burn extra power to ensure that the TRIAC does not misfire.

SACRIFICING EFFICIENCY

Burning extra power is contrary to the main goal of power-converter design: to provide efficient, well-designed, high-quality power processing. So the task for designers becomes twofold: to provide efficient power conversion from the ac mains to the LED load and to ensure that the phase dimmer functions properly while minimizing excess power loss.

New regulations for power quality now require PFC (power-factor control) for many LED systems. PF (power factor) is a measure of how well energy transfers from the input to the output of a converter. If the input current is free of distortion and perfectly in phase with the input voltage, the PF is one. Any phase shift or distortion of the input current due to reactive elements and switching noise decreases the PF.

Because most LED systems employ some form of PFC, the input current usually fairly well follows the input voltage, meaning that the phase dimmer usually misfires toward the end of the conduction angle where the voltage and current are decreasing (**Figure 2**). This misfire creates a varying angle decode, depending on where the misfire occurs.

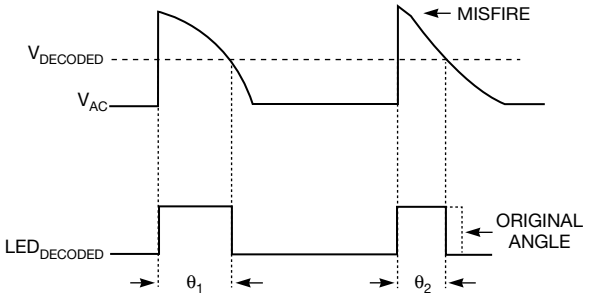

Figure 2 Most LED systems employ some form of PFC, which forces the voltage and current to stay mostly in phase. As a result, the phase dimmer usually misfires toward the end of the conduction angle where the voltage and current are decreasing and creates a varying angle decode, depending on where the misfire occurs.

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the holding-current requirement is to add a load resistance that ensures the design will meet the minimum input-current condition across the full conduction interval. This method is highly inefficient. For a 100W incandescent downlight replacement where only 15W of LEDs is necessary, this fixed hold current can cause a 10 to 20% efficiency drop.

A more complex approach is to linearly add the load every cycle, which involves ramping up the extra hold current during the conduction angle until it reaches the maximum at the end. This method can greatly reduce the efficiency drain; it is, however, difficult to design over a large operating range.

For example, in an 85 to 305V-ac universal input 15W LED downlight, the worst-case hold-current condition occurs at 305V ac, when the input current is at a minimum. To ensure that the TRIAC remains on over the entire conduction angle at 305V ac, you must add a fairly large amount of hold current. Because it is a universal design, the hold current you add at 85V ac would be approximately four times larger than necessary—a large waste of power.

DYNAMIC HOLD

The best way to maximize efficiency is to regulate the minimum input current. This approach draws no extra hold current when the input current is above the regulation point. Below the regulation point, the circuit draws enough current to maintain the minimum hold requirement. The LM3450 controller implements this method, called dynamic hold (**Figure 3**). A sense resistor between the diode-bridge return and system ground provides a method for input-current sensing. Using the sensed voltage across that resistor, the controller linearly draws current through the hold pin to maintain the minimum regulated input current. This ensures that any extra power dissipation is minimized.

Ultimately, the dynamic hold is necessary to ensure that the phase angle is being properly decoded to provide an accurate dimming command to the converter. The idea is to keep the TRIAC from misfiring during decoding so that the angle does not sporadically change, causing flickering. Looking closer at the system, it is actually unnecessary to decode the angle every cycle. A sampled system could provide even more efficiency relief. In this approach, the extra holding current would need to be added only during the sampling interval when decoding is taking place. During the nonsampled cycles, no current would be needed.

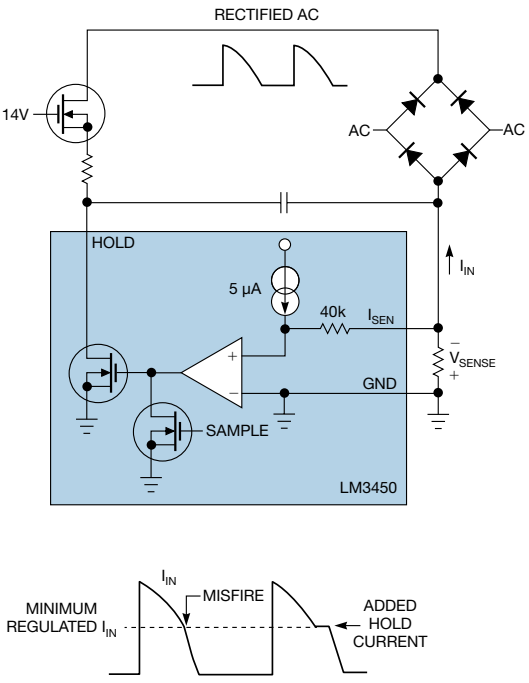

Figure 3 A dynamic-hold circuit draws no extra hold current when the input current is higher than the regulation point. Below the regulation point, it draws enough current to maintain the minimum-hold requirement.

The LM3450 employs this sampled-phase-decoder scheme, and the dynamic hold is thus active only during the sampling interval. To validate this approach, a 120V, 15W downlight application is implemented with both a fixed 20-mA holding current and a much larger 70-mA dynamic holding current (**Figure 4**). The 70-mA dynamic hold ensures a

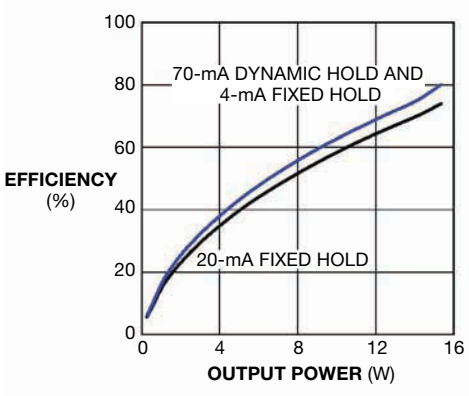

Figure 4 The results for a 120V, 15W downlight application using both a fixed 20-mA input load and a 70-mA dynamic hold show that the 70-mA hold ensures complete dimming range with more than 20 dimmers and yields an efficiency improvement of as much as 6%.

complete dimming range with more than 20 tested dimmers and yields an efficiency improvement of as much as 6%.

The designer has one difficult challenge using this approach. The previous analysis omits the impact of the EMI (electromagnetic-interference) input filter on the converter. Every converter requires filtering to pass standards regulating conducted and radiated EMI. Unfortunately, adding reactive components on the ac side of the rectifier bridge distorts the input-current measurement on the dc side. This problem becomes worse at the end of the conduction angle, when the dV/dt (rate of voltage change) of the input voltage is largest. At this point, the converter draws much of its current from the EMI capacitors, and the TRIAC conducts even less current than expected.

To deal with the sensing inaccuracy, the regulated minimum input current should be increased and the EMI filter capacitance minimized. EDN

AUTHOR'S BIOGRAPHY

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NETWORKING OVER POWER LINE: WILL NEXT-GENERATION TECHNOLOGIES STUMBLE

POWER-LINE NETWORKING HAS SO FAR SUFFERED NO SHORTAGE OF HICCUPS, YET ITS COMPELLING PROMISE REMAINS FUNDAMENTALLY UNTARNISHED. DO NEW TECHNOLOGIES MAKE NOTABLE ADVANCEMENTS OVER THEIR PREDECESSORS?

BY BRIAN DIPERT • SENIOR TECHNICAL EDITOR

In a 2007 article, I covered 200-Mbps-grade power-line technologies, which were then relatively new on the scene (**Reference 1**). The hands-on project examined three incompatible 200-Mbps power-line approaches: the Intellon-led HomePlug AV (audio/video), DS2's UPA (Universal Powerline Association), and the Panasonic-championed HD-PLC (high-definition power-line communication). It also analyzed earlier-generation, 14-Mbps HomePlug 1.0 and Intellon-proprietary, 85-Mbps HomePlug 1.0 Turbo, along with conventional Category 5e cabling and several variations of 802.11 wireless networking.

Much has changed in four years, during which I've periodically revisited multiple iterations of both HomePlug AV silicon and software upgrades (**Reference 2**). Intellon and Panasonic joined forces in developing the IEEE 1901 standard, which optionally supports HomePlug AV, HD-PLC, or both along with other feature enhancements. Atheros now owns Intellon, and Qualcomm now owns Atheros. DS2, which Marvell has acquired, redirected its technology attention toward the ITU's (International Telecommunication Union's) G.hn standard, which broadens the physical-transport options beyond the power grid to coaxial cable and twisted-pair telephone wire. Other acquisitions of power-line pioneers include Broadcom, which acquired Gigle Semiconductor; Sigma Designs, which purchased CopperGate Communications; and STMicroelectronics, which bought Arkados. Meanwhile, Infineon went in the opposite

IMAGE: CJ BURTON

OR SHINE?

direction, spinning off its networking group into a stand-alone corporate entity, Lantiq (see **sidebar** "Whither G.hn? Good question").

So it's a tempting time to revisit the power-line landscape. Although wireless networking is a natural candidate for untethered mobile-electronics devices, it's subject to range limitations, interference-induced degradation, and inherent performance shortcomings. Category 5e and coaxial cable—and, to a smaller degree, phone-line wire—deliver abundant bandwidth potential, but they restrict device location, and retrofitting a structure to enhance its wiring topology is time-consuming, expensive, and difficult. These shortcomings in part explain the inherent appeal of power-line networking: Why not take the same power cord you plug into a wall for electricity and use it for LAN and WAN (wide-area-network) connectivity? As you'll see, however, although power-line technology has made incremental progress from both speed and robustness standpoints, it's still not a panacea.

AT A GLANCE

- Ever-increasing bandwidth requirements couple with vendor consolidation and technology advancements to provide abundant motivation to revisit power-line networking.
- Ixia's IxChariot software suite proves capable of tackling both TCP (Transmission Control Protocol) and UDP (User Datagram Protocol) tests, in configurations with both single and multiple simultaneous streams.
- Atheros' latest IEEE 1901 chip set more than doubles the operating-frequency range of its HomePlug AV (audio/video) predecessors in striving to boost data-transfer speeds.
- Real-life XAV5001 performance improvements are sometimes slight and sometimes substantial. Unfortunately, these improvements often involve significant data loss in one case.

BENCHMARK BASICS

I chose open-source Iperf as the benchmark-testing utility of the earlier project (**Reference 3**). However, I later found that benchmarking projects are "fraught with potential peril" (**Reference 4**). Specifically, assumptions can heavily influence outcomes. A too narrowly focused choice of equipment, software, and usage model would be meaningful to only a narrow set of readers, whereas a broadly focused set of assumptions would yield a "bewildering plethora of outcome data." For example, altering just one variable, the TCP (Transmission Control Protocol) window size, dramatically boosted the measured bandwidth.

Fast-forward four years, and you'll find that Iperf has inherited other issues. The final 2.x-generation of the program, Version 2.0.5, which you can find on SourceForge, dates from mid-2010. There have been no further developments since, and, because its developers intended it primarily as a Linux application, finding up-to-date precompiled binaries for either Mac OS X or Windows is difficult to impossible. Version 2.0.0 of Jperf, the program's Java-based graphical front end, is even older, dating back to 2008. A reboot of the Iperf project, which the Google Code site hosts, is a new implementation with the goal of a smaller, simpler code base and a library version of the functions that you can use in other programs. Yet iperf3 is still in beta testing, and it's also not backward-compatible with iperf2.x.

As a result, I'm now using another common networking-benchmark utility, Ixia's IxChariot, which has worked out well. I had initially planned to use the company's freeware Qcheck program, but I ultimately found it too limiting. Qcheck's maximum data sizes yield tests that are too short to be statistically reliable. Qcheck supports only one TCP or UDP (User Datagram Protocol) stream, but I also wanted to simultaneously send multiple streams between

Figure 1 Ixia's Endpoint software runs on multiple operating systems, thereby enabling the use of a dual-core Mac OS 10.5-based MacBook in this project (a). My other Endpoint system, a dual-core Dell Latitude D420 running Windows XP Professional (b), did double duty as the foundation for Ixia's Console management-and-monitoring utility (c).

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WHITHER G.HN? GOOD QUESTION

Sigma Designs last fall had taped out on its CG5111-plus-CG5113 power-line-networking chip set and forecast that first silicon would become available by the end of 2010 (Reference A). As far as I know, the CG511x chip set is the first product to implement the ITU (International Telecommunications Union)-sanctioned G.hn networking standard. Sigma Designs also claims that it supports HomePlug AV (audio/video) and the IEEE 1901 follow-on, thereby enabling it to bridge the divergent standards. The company's proprietary ClearPath and ClearPath Extreme extensions allow for power-line packet transfer over not only the traditional phase-plus-neutral pair but also optionally instead using the power grid's earth connection. The extensions also enable simultaneous MIMO (multiple-input/multiple-output) broadcast and reception of multiple signals over multiple ac-wire pairs.

Early this year, I became aware of another planned G.hn silicon supplier, Lantiq, the former networking division of Infineon (Reference B). At the 2011 Consumer Electronics Show, Sigma Designs demonstrated initial CG511x silicon, and the company claimed that it hoped its firmware would be stable enough to ship samples to me by the end of February (Reference C). Similarly, Lantiq planned to obtain initial samples of its Xway HNX chip set from its fabrication facility in mid-March.

Despite these promises, this article omits both Lantiq and Sigma Designs. According to Michael Weissman, Sigma Designs' vice president of corporate marketing, the company was unable to provide the CG511x-derived adapters because G.hn-based products still required interoperability testing and other steps. The company instead sent three Motorola-branded adapters employing Sigma Designs' CG2110 HomePlug AV-only chip set. Similarly, Lantiq was not ready to ship samples as of late April, according to Chano Gómez, director of business development at the company.

Sigma Designs' CG2110 also supports ClearPath, and the Motorola adapters' three-plug configuration seemingly implements it, so I still plan to test these products. Nonetheless, G.hn was my fundamental motivation for engaging with both Sigma Designs and Lantiq. G.hn supporters are vigorous in their condemnation of HomePlug AV and its IEEE 1901 descendant, as UPA (Universal Powerline Association) backer DS2 had previously been. Yet, until the contenders deliver robust silicon, their words ring hollow. Meanwhile, Atheros and other IC suppliers, in partnership with system OEMs, will produce and sell ever-higher volumes of HomePlug AV and IEEE 1901 products, further increasing the technology's formidable worldwide dominance.

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any two network nodes as a way of measuring potentially increased aggregate throughput. Although Qcheck's TCP results are in the ballpark compared with those of IxChariot, Qcheck's UDP results significantly undershoot the UDP speeds that IxChariot measures. Qcheck also exposes substantially fewer testing variable dials to tweak, and it lacks scripting support.

IxChariot's Console utility, a Microsoft Windows application, sets up, manages, and periodically collects data from various tests. Qcheck also uses the companion network-node-resident utility, Ixia's Endpoint, which runs on Linux, Mac OS X, and Windows. Console comes with more than 100 company-created scripts, and users can both customize and copy scripts. As such, IxChariot has at least as many variables as Iperf—if not more. However, two premade scripts serve well for this project.

Because Console also bundles Endpoint, you can run Console from the same machine that acts as one of the tested network nodes. This combined setup is how I chose to conduct my benchmarking analyses (see **sidebar** "Head online for testing overtime," in the Web version of this article at www.edn.com/110623cs). However, according to Michael Githens, lab-programming manager at Ixia, this setup is not optimal for high-performance testing. Using the same CPU resources for both Console and Endpoint means that you may be unable to run either of them at full speed. Console and Endpoint functions are also contending for limited networking-transceiver bandwidth. Alternatively, you can run Endpoint software on two systems, with the Console utility executing on a third computer that communicates with the other two. In that case, the Console-installed PC can also have lower network performance than the others.

"It doesn't need a high-speed connection, [as the test links do]," Githens says. "It is passing less data; the results come only from the test links, not the management links."

TEST ENVIRONMENT

My approximately 1300-square-foot geodesic-dome residence dating from the mid-1980s serves as my test bed (**Reference 5**). Three of the power-line-network nodes I tested were in the approximately 25-foot-diameter downstairs main room, against one wall in a dining-room nook, in the middle of the room on a stairwell near the entertainment system, and against the opposing wall near the router. Next door to the router is the mud room, containing the fourth power outlet I employed in the testing, as well as the circuit-breaker box. I used another entertainment system in the upstairs bedroom as the fifth power-line node.

Each ac outlet connects to a phase of the 200V power feed, but I didn't know which phase or which circuit breaker each network node employed.

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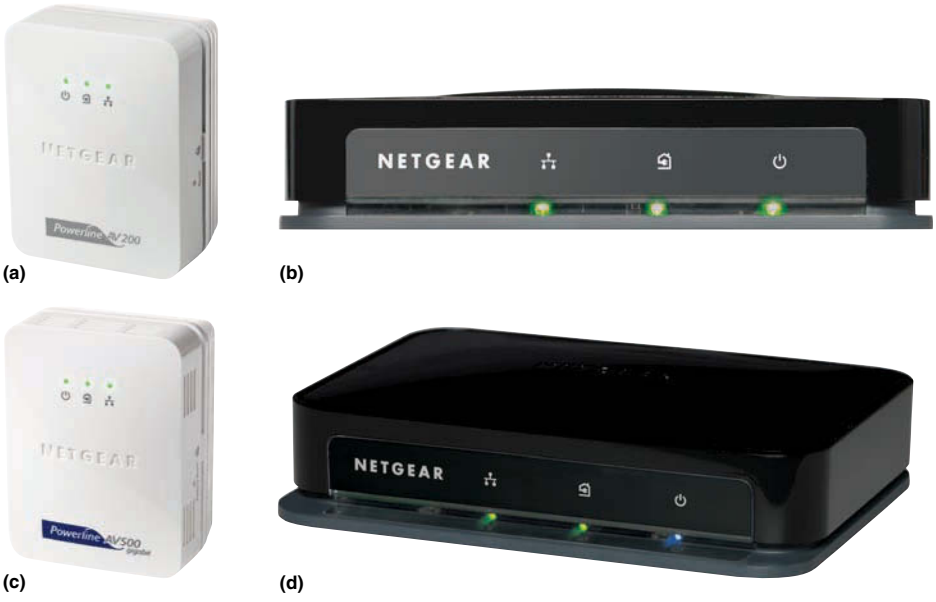


Figure 2 Netgear's single-port XAV2001 (a) and quad-port XAV1004 (b) adapters both employ Intellon (now Atheros) INT6400 chip sets. They have for several years formed the power-line foundation of my home-office LAN. I focused my benchmarking efforts on the XAV2001 for this hands-on study because only single-port XAV5001 successors (c) were available at the time. Subsequently, I've added quad-port XAV5004 adapters (d) to the day-to-day usage mix, with good results so far.

Having this knowledge would have been ideal because jumping across the phases at the circuit-breaker box can produce notably worse power-line-networking performance than that of network traffic that flows between same-phase outlets. And, when one circuit breaker feeds multiple same-phase outlets, they tend to deliver even higher bandwidth.

I employed various measures to minimize the effect of attenuation for these tests. As power-line-networking veterans know, packets don't pass through either surge protectors or UPSs (uninterruptible power supplies), so I ensured that such devices weren't between any of the power-line adapters and their associated power outlets.

Injected noise from running motors also kills packets. As a result, even though I normally have noise filters between my refrigerator's compressor and my home's furnace fan, neither they nor any other motors were operating when I was logging benchmark results. Using illuminated fluorescent bulbs is also a no-no if power-line-network performance is at a premium. One other noise-generating culprit might be a surprise to some: the switching power supplies in inexpensive ac adapters, battery chargers, and other wall-wart-based and otherwise ac-to-dc-fueled devices, so I unplugged them all before beginning the tests.

Because I was iteratively exercising multiple power outlets as network nodes throughout the house, I used portable computers as Endpoint-executing platforms. Most of my laptops and netbooks, however, contain only 10/100-Mbit Ethernet transceivers—a problem because some of the power-line-networking adapters embed GbE (gigabit-Ethernet) transceivers and claim greater-than-100-Mbps real-life performance. Fortunately, both a first-generation Apple MacBook, running Mac OS 10.5, and a Dell Latitude D420, using Windows XP Professional, offer the necessary 10/100/1000-Mbps Ethernet capabilities. The MacBook sufficed as an Endpoint, and the D420 also acted as a Console test bed after I confirmed through the task manager that simultaneously operating the Console and the Endpoint wouldn't swamp the Console's dual-core, 1.2-GHz processor (**Figure 1**).

ADAPTER CANDIDATES

I have for years run a combination of Netgear single-port XAV2001 and quad-port XAV1004 power-line adapters in my home LAN; the quad-port units integrate a switch. This setup has largely been successful, although I occasionally need to unplug and replug adapters to get them reliably talking to each other again (**Figure 2**). The XAV1004s are in my living-room- and bedroom-entertainment clusters, and the XAV2001s connect to my router and to a network-accessible Insteon controller with an embedded Web-server function. Thus, I'm simultaneously running power-line-based home-automation and networking traffic. The power-line-based equipment's modulation frequency is much lower than that of the networking traffic, however, so they don't interfere with each other. The XAV1004s and XAV2001s employ third-generation Atheros HomePlug AV silicon in the form of the INT6400 chip set. Testing confirms that they're both faster and more reliable than the second-generation INT6300 ICs in the Netgear XAV101 power-line-adapter predecessors.

The dining-room network node includes a Windows Vista Ultimate-based Dell XPS M1330 laptop. Through its Windows Media Center capabilities, the laptop (**Figure 3**) acts as an ATSC (Advanced Television Systems Committee) digital-television-antenna-array-fed PVR (personal video recorder). The XPS M1330 subsequently streams both live broadcasts and time-shifted recordings to the entertainment clusters' Xbox 360s, which act as Windows Media Center Extenders. The recording payloads, with approximately 20-Mbps bit rates, couple with real-life networking-technology bandwidth limitations, compelling me to construct a complicated networking topology. A dedicated, wide-channel, 5-GHz 802.11n wireless tether currently handles the XPS M1330-to-router span, and the router-to-game-console traffic

traverses over HomePlug AV. A second noninterfering, wide-channel, 5-GHz 802.11n beacon combines with a 2.4-GHz 802.11b/g access point to service general-purpose network packets.

I'm now using an ExpressCard-based single-tuner ATSC module in the XPS M1330 for TV reception. However, I've always wanted a dual-tuner setup. It would enable me, for example, to record one program while watching another or to watch two broadcast channels at once on two Xbox 360s. Realizing this aspiration would require a more robust laptop-to-router tether. Given that the SiliconDust HDHomeRun tuner I want to use is a stand-alone networked device, I'd also have to account for the equally formidable tuner-to-laptop-transfer-rate demands.

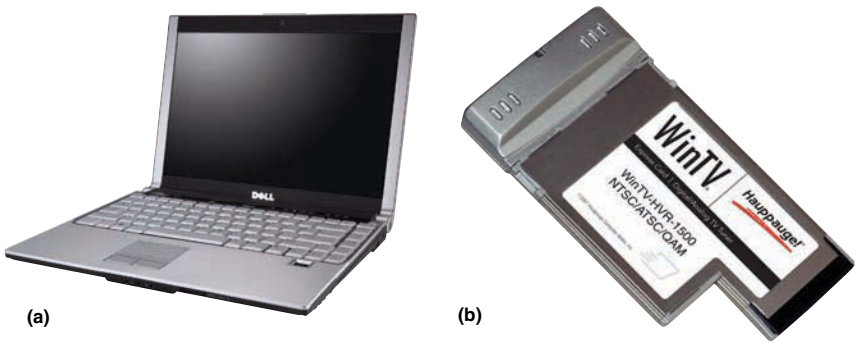
As such, Atheros' latest AR7400 PLC MAC (media-access-controller)/PHY (physical)-layer transceiver, with an AR1500 AFE (analog front end)/line driver, caught my eye. It claims to deliver more than 500-Mbps peak PHY rates—a 2.5-times improvement over alternative HomePlug AV products. It also claims peak PHY rates of 700 Mbps and as much as 350 Mbps of throughput over coaxial cables (**Reference 6**). Conventional HomePlug AV devices operate over a frequency range of approximately 2 to 28 MHz, minus notch-filter-suppressed bands, to avoid interference with short-wave-radio equipment. The AR7400/AR1500 combo, conversely, extends the operating-frequency range to the optional IEEE 1901-specified 68-MHz threshold.

This approach is conceptually similar to that of Gigle Networks' GGL541-based Belkin adapters, which I have used, although the implementations differ somewhat. The GGL541 dynamically selects between a 2- to 28-MHz frequency band for conventional HomePlug AV operation and a 50- to 300-MHz band for the company's proprietary Mediaxtream technology. The AR7400 chip set, conversely, employs a unified 2- to 68-MHz spectrum swath, minus the notch filters.

The AR7400 chip set can route power-line-networking traffic over the earth-ground connection between adapters instead of using the conventional phase-plus-neutral-wire pair—if a performance or another advantage to doing so exists. As such, its SmartLink implementation is conceptually similar to the ClearPath capabilities that Sigma Designs' HomePlug AV-plus-G.hn-CG5111-plus-CG5113-chip-set arrangement touts (**Reference 7**). Achieving this silicon potential, however, requires three-prong power-line adapters; by press time, Atheros and its OEM partners could provide only two-prong units (**Figure 4**). Ethernet wiring also involves concerns: To connect a power-line adapter to either the router or a computer, I employed the 8-foot cables that came with the XAV5001 units, assuming that Netgear had supplied wiring of sufficient quality to avoid hampering the adapters' performance.

TESTING RESULTS

When I did my benchmarking, I had access only to single-port XAV5001s—not to Netgear's XAV5004 four-port,



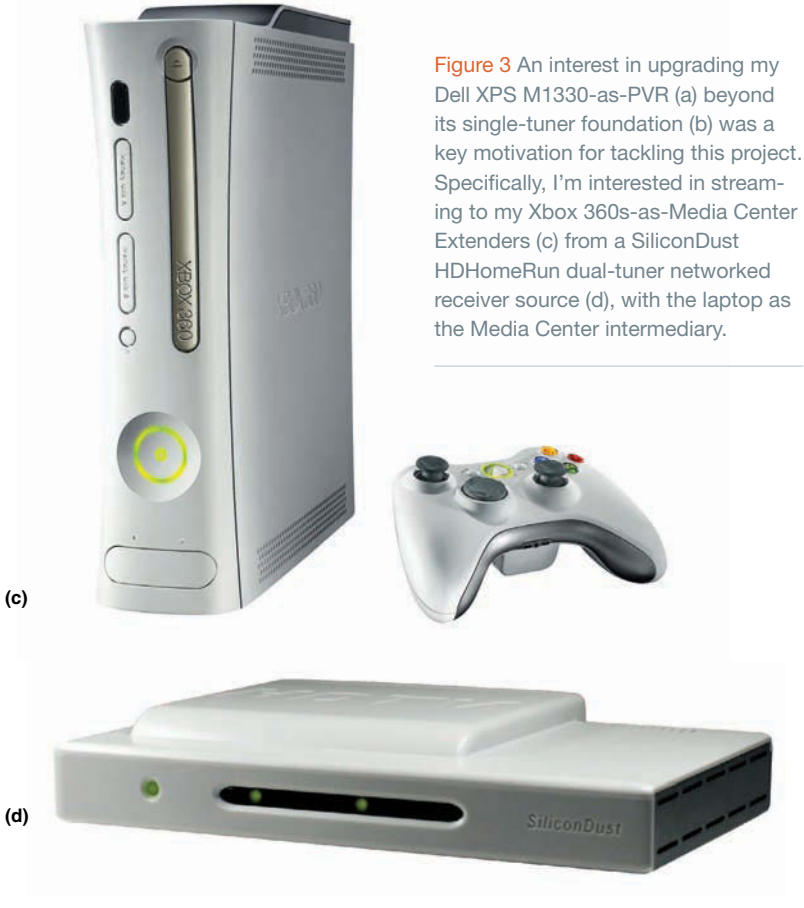


Figure 3 An interest in upgrading my Dell XPS M1330-as-PVR (a) beyond its single-tuner foundation (b) was a key motivation for tackling this project. Specifically, I'm interested in streaming to my Xbox 360s-as-Media Center Extenders (c) from a SiliconDust HDHomeRun dual-tuner networked receiver source (d), with the laptop as the Media Center intermediary.

AR7400-based IEEE 1901 adapters. So I swapped out my XAV1004 AR6400-based HomePlug AV units for XAV2001 adapters to create an apples-to-apples comparison. The testing results show bandwidth variability—both from one node combination to another and, within a node combination, from one data-flow direction to another (**Table 1**). Note that the simultaneous transfer of four TCP or UDP streams sometimes delivers higher aggregate bandwidth than does a single-stream protocol.

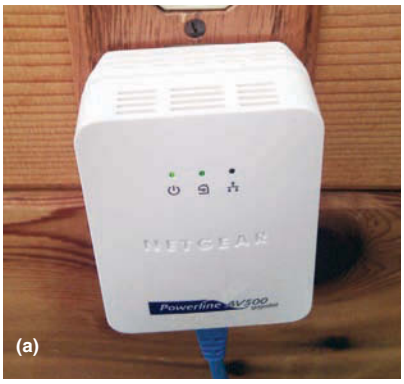
For testing, I chose the four-stream test supplement to the single-stream base-case test after reviewing past benchmarking projects from SmallNetBuilder, a highly regarded online networking-evaluation site, which also uses IxChariot. Following in SmallNetBuilder's footsteps, I modified Ixia's bundled Throughput.scr IxChariot script for both single- and four-stream TCP testing, changing the per-stream test-data payload size from 100 kbytes to 1Mbyte.

Expanding beyond SmallNetBuilder's TCP-centric approach, I also ran single- and four-stream UDP tests. Four-stream UDP testing employed Ixia's UDP_Throughput.scr IxChariot script as is, whereas I modified UDP_Throughput.scr for single-stream UDP tests to increase the per-stream data-payload size from 730 kbytes to 7.3 Mbytes to lengthen the test's runtime.

For TCP-focused benchmarking, I successfully initiated tests from the Console system. These tests sent data from the Console-running laptop to the Endpoint-running laptop, and vice versa. Conversely, for UDP-focused benchmarking, I could reliably stream data only from the Console-based laptop to the Endpoint-running laptop, resulting in notably increased time and effort between tests for shuttling systems to various nodes. During all of the tests, I plugged in all five nodes' power-line adapters, although only the two that connected to the Console and Endpoint laptops and the one tethered to the router were passing any network traffic.

Note the results I obtained when I replaced all of the INT6400-based Netgear XAV2001 HomePlug AV adapters with AR7400-based, IEEE 1901-compatible Netgear XAV5001 alternatives in the same locations and orientations as their predecessors. The XAV5001 adapters occasionally had trouble establishing connection with each other, and, even if they did initially sync up, they'd sometimes drop the handshake a short time later. Both are undesirable scenarios, to which the adapters' front panels' red lights would alert me. I would try to mitigate the situation by unplugging and then plugging back in the offending adapters. The XAV2001 predecessors didn't seem to suffer from this communication breakdown. When the XAV5001s were in sync, however, their performance was impressive—most of the time, at least.

In rerunning all of the tests, I frequently obtained speedier—sometimes dramatically speedier—transfer rates with the XAV5001s than with the XAV2001s. Keep in mind that **Table 1** shows only the average throughput across each test's duration. Each single-number test summary omits per-stream average results for four-stream tests; the minimum and maximum per-stream and aggregate transfer rates across the test runtime; the overall transfer-rate pattern spread; and the measured minimum, maximum, average, and spread



(c)

Figure 4 Two-prong power-line adapters offer outlet location (a) and orientation flexibility (b) that may unfortunately also result in reliability and performance degradation versus three-prong alternatives (c).

latency. The IxChariot reports embed all of this information and more. You can download this information in both native Ixia TST (test) and exported HTML (hypertext-markup-language)-format-plus-GIF (graphic-interchange format) from http://briansbrain.wordpress.com.

Table 1 also shows packet-loss results for the quad-stream UDP tests of the XAV5001 adapters. With all other tests, spanning both power-line-adapter technologies, both protocols, and both single- and four-stream test scenarios, source-to-destination data-transfer success rates were consistently greater than 99% and, frequently, 100%. However, in these cases, the packet loss is substantial and repeatable. I reran the tests multiple times over the course of many days. Again, the worst-case stream's four-stream average loss was sometimes notably higher than that of the four-stream average.

DROPPED-PACKET DIAGNOSIS

I don't typically share testing results with vendors before an article's publication, but this case seemed atypical. To ensure that I wasn't overlooking some fundamental mistake that would unfairly represent Atheros and Netgear's partnership product, I informed Atheros and Ixia that I had encountered approximately 50 to 75% data loss only in my four-stream UDP tests and only with the AR7400-based adapters. However, I did not provide Atheros with per-test statistics.

Peter Shread, senior manager for PLC-application engineering at Atheros, immediately got on the case, attempting to duplicate my results after first confirming that I was running the latest XAV5001 production-firmware revision. Shread subsequently stated that Atheros could not replicate the packet loss that I had reported. The company tested with a pair of the XAV5001s, as well as a set of AR7400 reference-design adapters, all running the same firmware version I had used. The company set up the test with 20 dB of attenuation between the two adapters and transmitted one, two, four, and six UDP streams. The testers observed less than 1% packet loss, and the streams' aggregate throughput was approximately 250 Mbps in all cases.

I later received a multipage foil set detailing the company's testing method and results (**Figure 5**). In further explaining the test-bed setup, the company performed testing on a clean line with 20 dB of attenuation as well as on a power-line setup to simulate typical in-home loads, according to Shread.

There are a few possible explanations for why my quad-stream UDP testing results differ so radically from those of Atheros. One reason might be that every setup is unique, and the company's simulation may not encompass some nuance of a real-life setup. Alternatively, although I attempted to squelch both other network traffic and spurious power-grid noise from other devices, perhaps I had overlooked an offending device. Also, in power-line-networking-equipment testing, results can depend on which power outlet you use in a multiple-outlet cluster and on the orientation of the adapter in the outlet. In

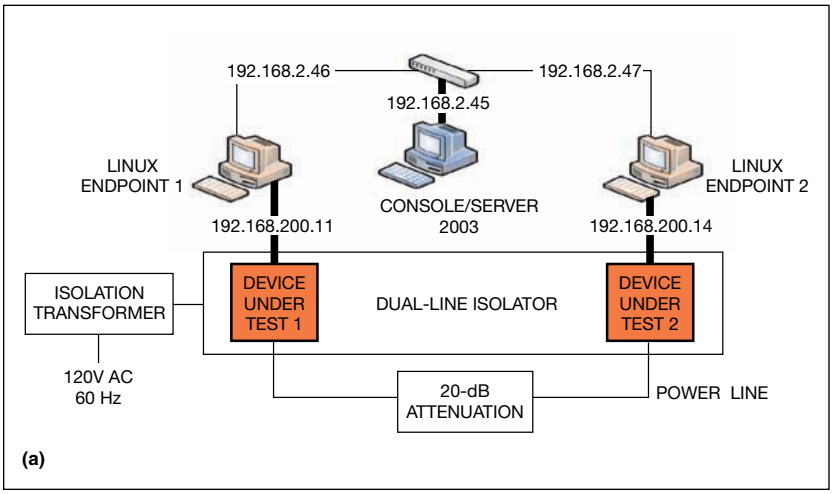
TABLE 1 POWER-LINE-ADAPTER TESTING RESULTS

	Netgear HomePlug AV[1]			
	Single-stream TCP	Quad-stream TCP	Single-stream UDP	Quad-stream UDP
Dining room to living room	38.27	39.04	38.329	40.812
Living room to dining room	34.034	35.943	40.571	39.414
Dining room to bedroom	30.947	32.351	39.237	37.805
Bedroom to dining room	30.861	32.688	35.378	34.674
Dining room to mud room	37.427	35.465	38.149	36.362
Mud room to dining room	35.197	36.006	41.148	40.856
Living room to bedroom	44.946	46.717	40.567	57.921
Bedroom to living room	44.576	49.63	41.714	60.136
Living room to mud room	50.952	60.914	41.95	69.202
Mud room to living room	53.652	57.227	40.715	70.681
Bedroom to mud room	48.074	55.672	41.408	64.991
Mud room to bedroom	47.818	50.318	41.697	62.956
	Netgear IEEE 1901[2]			
	Single-stream TCP	**Quad-stream TCP**	**Single-stream UDP**	**Quad-stream UDP**
Dining room to living room	50.936	48.376	40.273	55.846 (67.427% loss)
Living room to dining room	53.38	47.199	41.1	66.891 (62.104% loss)
Dining room to bedroom	40.883	41.737	40.883	45.074 (73.417% loss)
Bedroom to dining room	42.664	44.219	42.664	56.893 (67.241% loss)
Dining room to mud room	37.958	37.306	40.589	44.981 (73.706% loss)
Mud room to dining room	42.317	38.397	38.97	49.570 (70.916% loss)
Living room to bedroom	64.18	62.048	64.18	76.004 (55.953% loss)
Bedroom to living room	67.002	65.139	67.002	69.783 (59.101% loss)
Living room to mud room	81.202	87.142	40.014	100.167 (43.223% loss)
Mud room to living room	66.957	84.157	40.751	99.855 (45.033% loss)
Bedroom to mud room	60.689	68.707	60.689	86.659 (50.149% loss)
Mud room to bedroom	66.286	74.795	66.286	88.850 (49.109% loss)

[1]Firmware vINT6000-MAC-4-0-4011-01-3431-20090519-FINAL
[2]Firmware vINT7000-MAC-5-0-5010-02-655-20101100-FINAL

my tests, for example, the dining-room node employs a right-side-up adapter residing in the lower outlet of the two-outlet cluster (**Figure 4a**), whereas all other nodes' adapters are upside-down and in the upper outlet (**Figure 4b**).

Another possibility could be that Atheros used different Endpoint and Console computers running different operating systems from those that I used. Alternatively, note that all of the computers on Atheros' test beds had



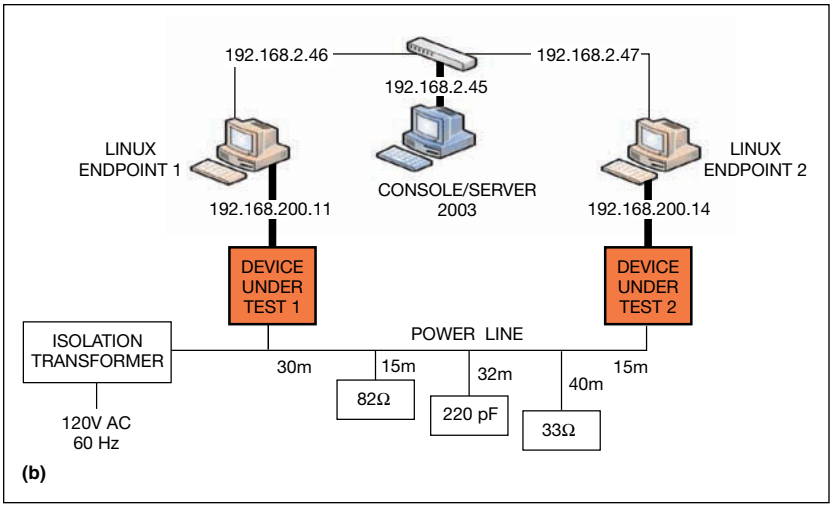


Figure 5 Concerns over quad-stream UDP's substantial data loss on AR7400-based adapters prompted Atheros to attempt to replicate my testing results using a combination of a clean-line setup with in-line attenuation (a) and a more complex test bench, which the HomePlug Forum has approved for certification purposes, to simulate typical in-home loads (b). SiliconDust's latest triple-tuner networked receiver provides justification for multistream robustness (c).

static IP (Internet Protocol)-address assignments and therefore interconnected using only a switch, whereas my setup employed DHCP (Dynamic Host Configuration Protocol) assignments and therefore interconnected using a power-line-adapter-fed router.

One of the two Endpoint computers in my setup also acts as the Console system, whereas Atheros dedicated a third computer to the Console management-and-monitoring function. And, with Atheros' setup, IxChariot management traffic ran between the Console and the Endpoint systems over a dedicated Category 5-implemented network (192.168.2.xxx); a second Ethernet adapter in each Endpoint system handled power-line-test-packet flow between them (192.168.200.xxx). In my setup, both test and minimal management traffic flowed over the power-line network.

Using four simultaneously running UDP streams for a power-line adapter, although probably not a common scenario, is by no means infeasible. Consider, for example, the SiliconDust dual-tuner networked-TV receiver, which uses the LAN to connect to a Windows Media Center-based computer. This computer also connects with two Media Center extenders. If both the HDHomeRun and the computer connect to the network using power-line adapters and if both tuners are active at once, two UDP streams' worth of information flows from the HDHomeRun's adapter to the computer.

Further, Media Center extenders elsewhere in the home could simultaneously be viewing those two streams or others, such as prerecorded content. In this case, two more streams are flowing in opposite directions through the computer's power-line adapter. Considering that SiliconDust recently released three- and six-stream networked receiver appliances, my four-stream UDP scenario is looking more mainstream all the time.

Soon after completing benchmark tests, I received two four-port Netgear XAV5001 adapters, so I upgraded the power-line portion of my LAN to AR7400-based adapters—a mix of XAV5001s, replacing the XAV2001s, and XAV5004s, replacing the XAV1004s. This setup operated for weeks without glitches, but I haven't yet tried a usage scenario with more than one UDP stream. I plan to do more testing to find out whether the issue is a tool-set, silicon, or usage shortcoming or some combination of these variables. EDN

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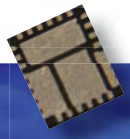

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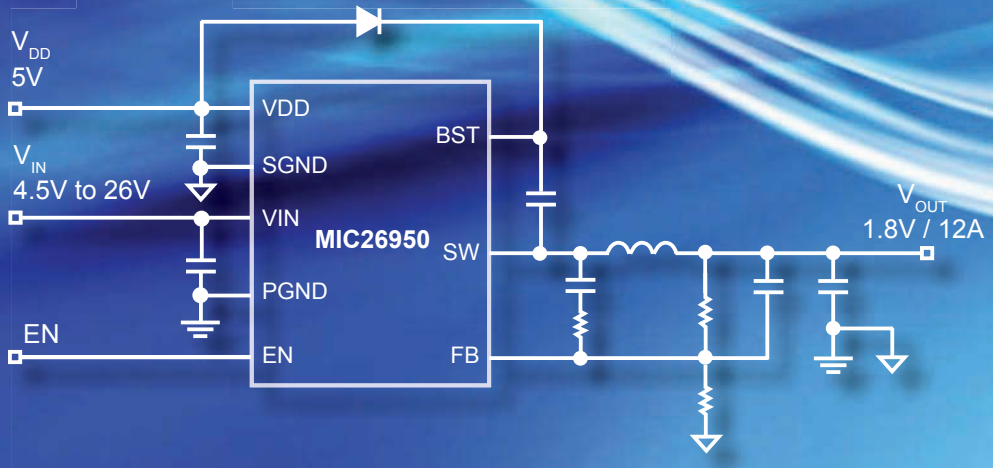

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READERS SOLVE DESIGN PROBLEMS

Protect power-LED strings from overcurrent

Luca Bruno, ITIS Hensemberger Monza, Lissone, Italy

A common method for driving multiple power LEDs is through two parallel strings. This inexpensive and less critical driver circuit can provide a lower voltage. However, the driver circuit must deliver twice the current of other methods and needs a circuit that halves the current in the two strings, regardless of the LEDs' forward voltages. The LEDs' forward-voltage tolerance is as high as 20%, and the voltages change with LED temperature and aging.

A current mirror performs this task well. If an LED breaks, it can cause destructive overcurrent. The current mirror, however, can safely partially protect two parallel, connected strings of any number of 350-mA power LEDs from these overcurrents (**Figure 1**).

The circuit can balance the currents between strings with a matching error of approximately 2% because of the equal voltages of 0.5V developed on 1.5Ω emitter resistors R_1 and R_2 with 1% tolerance. The voltage drop across resistor R_3 compensates for the mismatching of LED voltage drops and holds both Q_1 and Q_2 in the linear region. The voltage drop depends on how many LEDs make up the two strings.

If an LED of String 2 fails, however, no base current flows to transistors Q_1 and Q_2, and they turn off. All LEDs in String 1 have automatic overcurrent protection. The circuit doesn't perform the same function if an LED in String

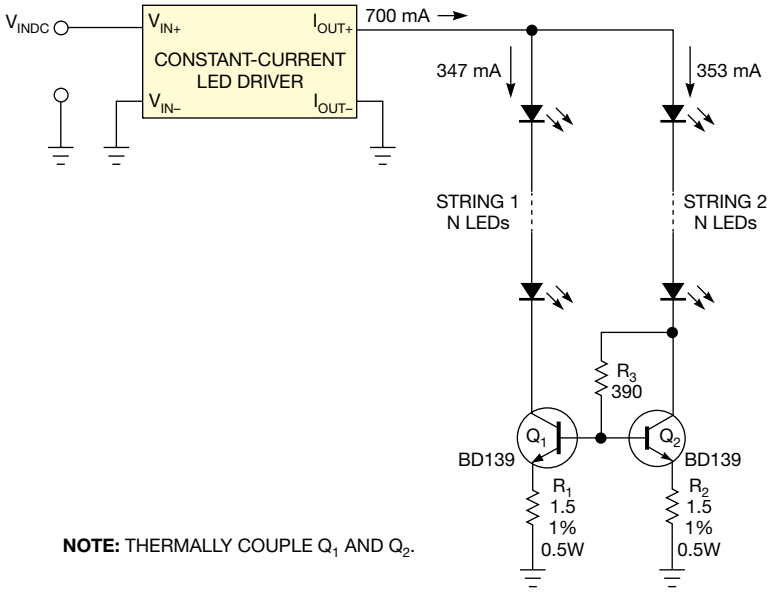

Figure 1 Using a current mirror, you can safely protect two parallel, connected strings of any number of 350-mA power LEDs from destructive overcurrents.

DIs Inside

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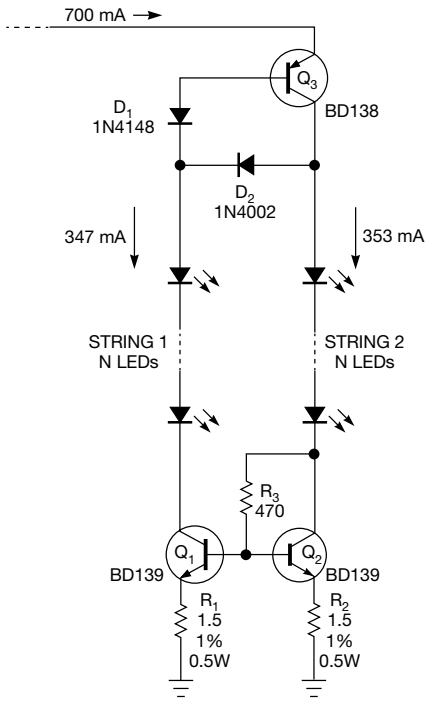

Figure 2 An LED in String 1 can fail because all of the 700-mA driver current flows into String 2, which needs some form of protection. You can solve this problem by adding only three components.

1 fails because all of the 700-mA driver current flows into String 2, which needs some form of protection. You can solve this problem by adding only three components (**Figure 2**).

In normal operation, transistor Q_3 operates in its linear region with an emitter-collector voltage of 0.7V because both diodes D_1 and D_2 are forward-biased. The power dissipation of Q_3 is only about 0.5W, and it thus needs no heat sink. The 700-mA driver current coming from the collector of Q_3 divides equally between the strings through steering diode D_2, as the current mirror dictates. If an LED in String 1 fails, diode D_2 blocks the base current of Q_3, turning it off. The driver current can no longer flow through String 2, safeguarding the LEDs.

You must compensate for diode D_2's 0.7V voltage drop, which slightly increases the value of resistor R_3. You can adapt the current mirror for driving any type of LED without exceeding the absolute maximum rating of the transistors' collector current, which is 1.5A. You can test the current mirror with any 700-mA constant-current LED driver, or even a voltage regulator configured as a current source, such as National Semiconductor's (www.national.com) LM317 regulator. The circuit underwent testing, with the LM317 acting as a 700-mA current source with five LEDs per string. EDN

Simple flasher operates off ac mains

Noureddine Benabadji,
University of Sciences and Technology, Oran, Algeria

Looking for a mains switch in the dark is easier if the switch contains a built-in neon or filament miniature lamp. Adding a small indicator to any mains switch is helpful. It is even better if the indicator flashes. This circuit makes a simple flasher using only four discrete components (**Figure 1**).

The neon lamp flashes at a frequency of 1 to 5 Hz, according to experimental values for resistance and capacitance. When the switch terminals are open, diode D_1 acts as a half-wave rectifier. Capacitor C_1 charges through resistor R_1 until the voltage on the capacitor exceeds the breakdown voltage of a miniature neon lamp. C_1 then discharges rapidly through the lamp, which flashes. You can access the switch terminals by prying off the front panel with a small screwdriver. This circuit can be installed inside the switch block. You assemble it on a 5×10-mm PCB (printed-circuit board).

This flasher circuit works properly only with 220V tungsten lamps. To use it with 220V fluorescent lamps, you must make a small modification (**Figure 2**). Disconnect resistor R_1 from the flasher circuit and place it in parallel with the starter of the fluorescent lamp, which is connected in series with the mains switch. EDN

THIS CIRCUIT MAKES A SIMPLE FLASHER USING ONLY FOUR DISCRETE COMPONENTS.

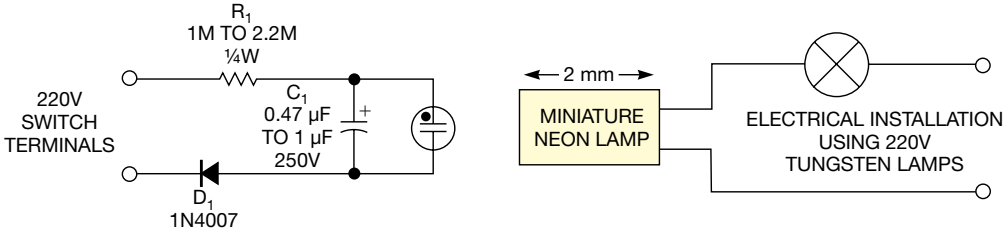

Figure 1 You can add this simple flasher inside a mains switch.

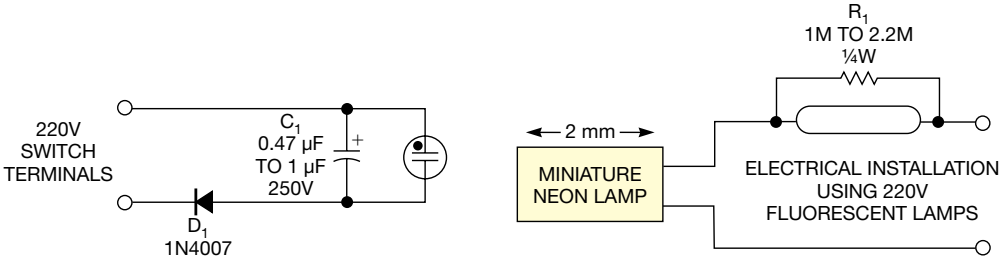

Figure 2 Use this modified circuit to operate with fluorescent lamps.

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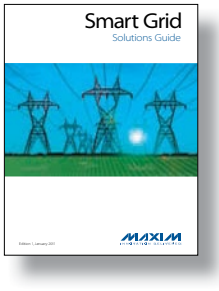

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Use resistor noise to characterize a low-noise amplifier

Joe Geller, Whitesboro, NY

If you know or can estimate a low-noise amplifier's gain or noise bandwidth, you can measure the other spec using only a handful of resistors and an ac voltmeter (**Reference 1**). The method in this Design Idea uses the Johnson Equation, which describes the amount of noise a resistor generates (**Reference 2**). To find the missing parameter, measure an amplifier's output-noise voltage, first for a shorted input and then using a few resistors of different values. You can download an Excel spreadsheet that can calculate gain or noise bandwidth from the online version of this Design Idea at www.edn.com/110623dia.

To begin the measurement, place a short circuit across the low-noise amp's input terminals and measure the noise voltage with the voltmeter. Next, insert the resistors, one at a time, across the amplifier's inputs and measure the noise voltage at the output of the amplifier. Enter the measured output-noise voltages, the measured values of each resistor's resistance, the ambient temperature, and either the known or the estimated gain of the low-noise amp or the known or estimated effective noise bandwidth into the spreadsheet.

Using each of the measured resistance values, the spreadsheet plots a theoretical "blue" curve representing the Johnson noise in normalized units of nV/√Hz (**Figure 1**). You can compensate

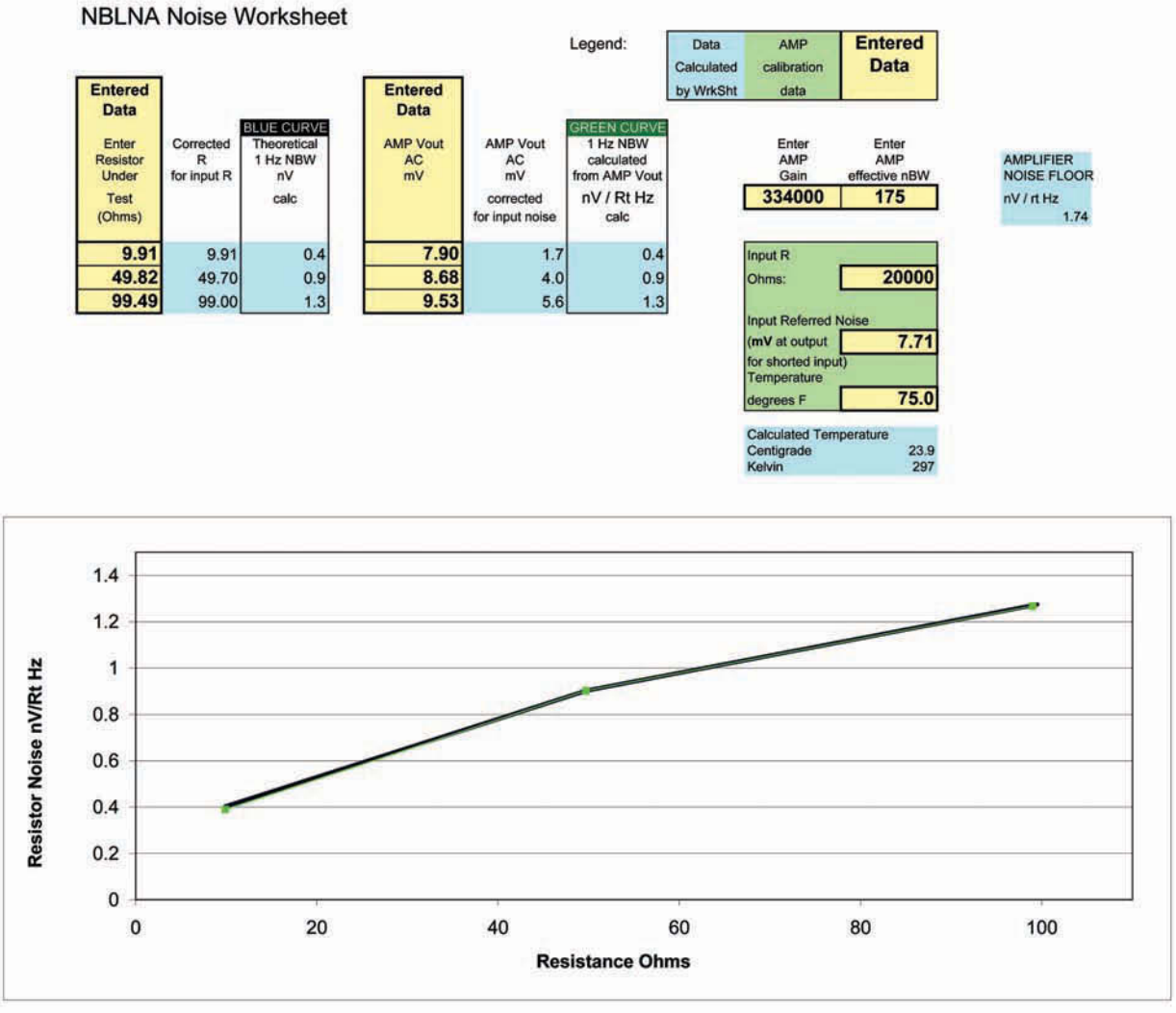

Figure 1 This downloadable spreadsheet lets you characterize an amplifier's gain and noise.

the blue curve for any low-noise-amp input resistance. The graph also shows a "green" curve that represents the amplifier's calculated "excess" output noise—the measured output minus the amplifier's uncorrelated input-referred noise. The input-referred noise is an uncorrelated noise signal that adds to any excess input noise as the square root of the sum of the squares of the noise voltages. You can find the amplifier's input-referred noise using its effective-noise-bandwidth and gain values and measuring the output-noise voltage by short-circuiting the amplifier's input terminals.

You can use a multimeter, such as Agilent's (www.agilent.com) 34410A, with a second-display math-average feature to fill in the measured output-noise values (**Reference 3**). After you connect each resistor to the amplifier's input terminals when the amplifier is on, reset the math average; wait until the new value settles down, which typically takes 10 seconds to approximately one minute; and record the average value for that resistor on the noise worksheet. Use the ohmmeter function to measure the actual resistance value and enter that value into the spreadsheet.

Enter the input parameters and measured output-noise values into the spreadsheet. Take a guess at the unknown parameter's initial value and then vary it until the green curve almost exactly overlaps the theoretical blue curve. When the curves overlap, you've found the missing parameter. You can then try what-if scenarios by varying both parameters. EDN

A MULTIMETER HAS A SECOND-DISPLAY MATH-AVERAGE FEATURE THAT CAN BE USED TO FILL IN THE MEASURED OUTPUT-NOISE VALUES. USE THE OHMMETER FUNCTION TO MEASURE THE ACTUAL RESISTANCE VALUE.

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Build a UWB pulse generator on an FPGA

Punithavathi Duraiswamy, Xiao Li, Johan Bauwelinck, and Jan Vandewege,
Ghent University, IMEC/Department of Information Technology, Ghent, Belgium

You can implement a digital UWB (ultrawideband) pulse generator in most FPGAs. The design lets you create a pulsed signal with a frequency that's twice the FPGA's clock frequency (**Figure 1**). A previous design relies on asynchronous delays to make pulses of the desired frequency. That design, however, requires an FPGA that supports tristate pullups, such as the Xilinx (www.xilinx.com) Virtex 2 (**Reference 1**). That approach also requires manual placement and routing. Today's FPGAs don't support tristate pullups. In addition, asynchronous delays vary with temperature. This Design Idea uses a synchronous-delay approach employing a combination of multiple clock phases. You can implement this design in all types of FPGAs.

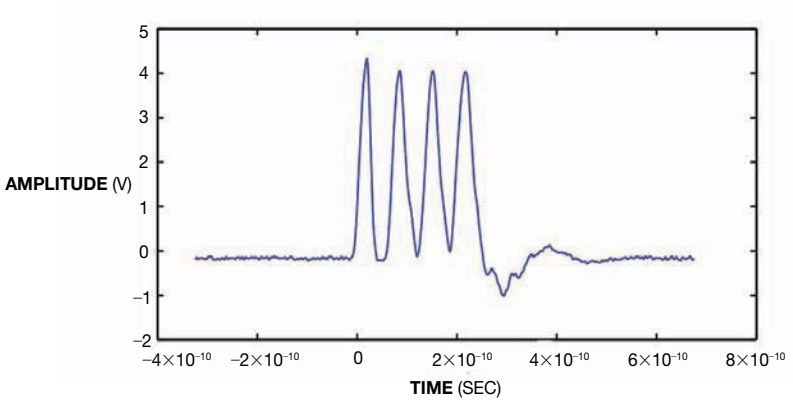

Figure 1 A pulse's frequency reaches twice the FPGA's clock frequency.

The maximum clock frequency of the DCM (digital clock manager) and the flip-flops are the main limiting factors in this design. For example, the DCM of a Xilinx Virtex 4 can't exceed 400 MHz. An FPGA can generate signals of frequencies that are half the clock frequency because it takes two clock pulses to toggle the signal from zero to one and back. Thus, you can't directly generate frequencies greater than half the clock frequency. This design lets you generate pulsed signals higher than half the clock frequency and reaches twice the clock frequency by using multiple clock phases from the DCM and synchronous delays smaller than one clock period.

Figure 2 shows the proposed pulse generator. It consists of three functional blocks, an OOK (on/off-key) modulator, a synchronous-delay generator, and an edge combiner comprising an exclusive OR gate. The OOK modulator comprises an inverter that the pulse-repetition-frequency signal triggers at every start of a new pulse. When a trigger occurs, the OOK circuit inverts a preinitialized signal to a time equal to a count value derived for a pulse width and remains zero until the next trigger. The OOK block generates a frequency that is one-half the clock frequency. This OOK output passes through the synchronous-delay generator, which generates three delayed versions of the OOK output.

These delays are smaller than one clock period. The clock phases in turn clock flip-flops FF_1, FF_2, and FF_3, which lag by 90, 180, and 270°, respectively. These delayed pulses then combine with the output of the OOK modulator using combinatorial logic to generate the desired frequency for the UWB pulses. The edge combiner performs an XOR (exclusive-OR) operation, which generates signal frequencies that depend on the edges you want to combine. Combining the output of the OOK edge with the output of FF_1 generates a signal frequency equal to the clock frequency. Combining the edges of all outputs generates a signal frequency equal to two times the clock frequency. The DCM synchronizes these

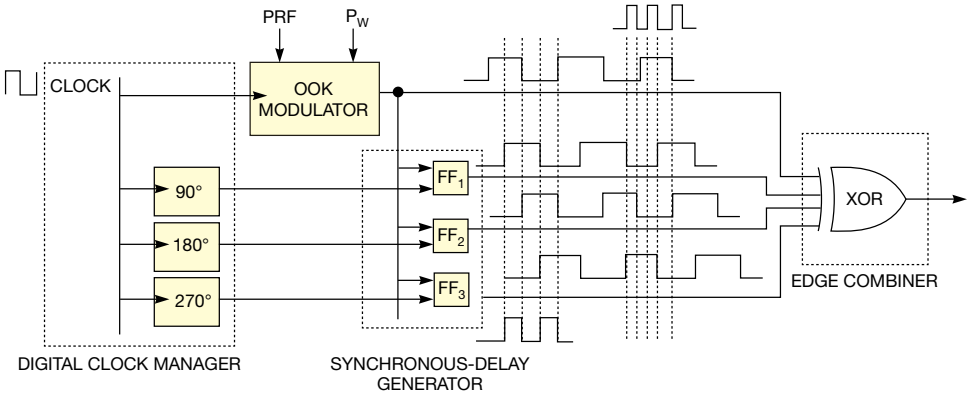

Figure 2 The design uses an OOK modulator, a clock manager with three phase shifters, three flip-flops, and an exclusive OR gate.

delays, producing an accurate signal frequency. This design is less complex than the asynchronous-delay approach in **Reference 1**.EDN

REFERENCE

1 Park, Youngmin, and David D Wentzloff, "All-digital synthesizable UWB transmitter architectures," *Proceedings of the 2008 IEEE International Conference on Ultra-Wideband*, Volume 2, 2008, http://bit.ly/j3wVuG.

Generate swept sine/cosine waveforms with two filters

John R Ambrose, Mixed Signal Integration, San Jose, CA

Demodulators, directional circuits, and other electronics applications often need two sine waves with a 90° difference in phase—a sine wave and its cosine wave. Engineers typically use analog filters to create the phase shift. This approach, however, offers a limited frequency range. Using the circuit in **Figure 1**, you can make a swept sine/cosine pair at frequencies of less than 1 Hz to 25 kHz.

The Mixed Signal Integration (www.mix-sig.com) MSFS5 selectable lowpass/bandpass switched-capacitor filter removes the harmonics from a square wave you apply to its inputs. The clock for the MSFS5 is 100 times the input square wave. The 74HC390 and 74HC74 form a divide-by-25 and a divide-by-two circuit. The Q outputs from the 74HC74 connect to the two divide-by-two circuits in the 74HC390A, which produces square waves that are 1/100 of the filter clock's frequency and are 90° out of phase from each other. A square wave at CMOS levels would saturate the filter, so the circuit uses resistor dividers R_1 through R_4 to reduce the signal's amplitude.

Figure 2 shows the output of the two filters at 20 kHz with a system clock of 2 MHz. Note that the phase reading on the scope is at –89.85°. When swept in frequency, the phase varies from –89 to –91°. **Figure 3** shows a 20-kHz Lissajous pattern.

Measuring the circuit's distortion using a spectrum analyzer and an Audio Precision (www.ap.com) audio analyzer shows a THD (total harmonic distortion) of –49 dB. Testing shows that the circuit has no discontinuity at the filter outputs with either FSK (frequency-shift keying) or FM (frequency modulation).EDN

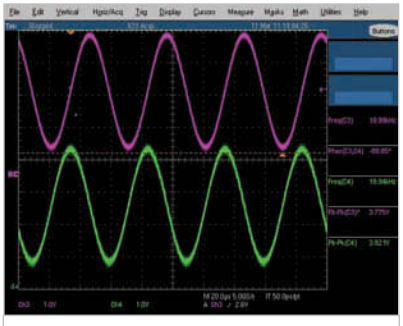

Figure 2 The phase reading on the scope is –89.85°.

Figure 3 When swept in frequency, the phase varies from –89 to –91°.

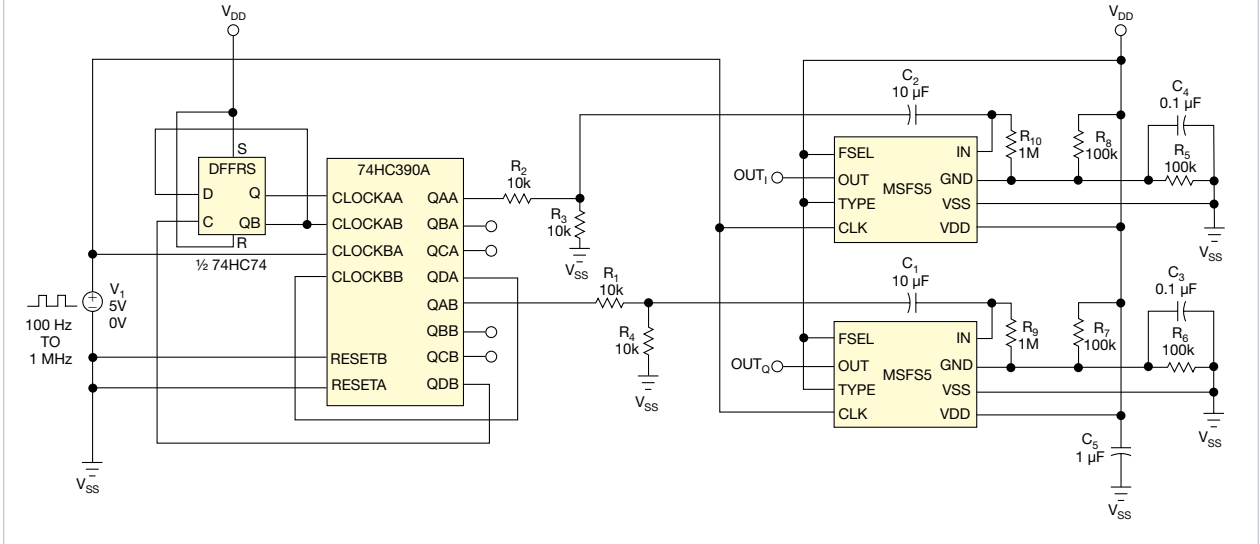

Figure 1 This circuit lets you make a swept sine/cosine pair at frequencies of less than 1 Hz to 25 kHz.

productroundup

MOTION

Evaluation platform drives three-phase brushless motors

The DRV8312-C2-Kit motor-control evaluation kit spins less-than-50V, 6.5A brushless-dc and permanent-magnet-synchronous motors for driving medical pumps, gates, lifts, and small pumps, as well as industrial and consumer robotics and automation. The product includes the DRV8312 motor driver, a 32-bit C2000 Piccolo microcontroller-control-card module, a quick-start graphical user interface, full development source code, the Code Composer Studio integrated development environment, and a three-phase brushless-dc motor. The evaluation kit sells for $299.

Texas Instruments, www.ti.com

Piezoresistive pressure transducer features high intensity

The miniature high-sensitivity Endevco model 8510B piezoresistive pressure transducer is available in sensitivities of 200, 500, and 2000 psig with a 300-mV full-scale output. The four-active-arm-strain bridge-and-silicon-diaphragm design has integral temperature compensation of –18 to +93°C (0 to 200°F) for accuracy over the full temperature range and a nonlinearity of less than 1% at a three-times overrange. Units offer high resonance frequencies for accurate measurements over the full audio range. Prices start at $1020.

Meggitt Sensing Systems,
www.meggittsensingsystems.com

Design tool assists in motion-device selection

A downloadable motion-control design tool assists users in selecting the vendor's smart power modules. The tool addresses three-phase inverter sinusoidal modulation for variable-speed-drive applications powering permanent-magnet-synchronous motors and ac-induction motors. It bases selection on a detailed entry of application-specific I/O information. The program's output includes module-component losses, junction-temperature increases, cooling requirements, and junction-temperature ripple at the motor/output frequency. Users can launch the tool

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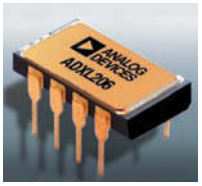
from www.fairchildsemi.com/design_tools/motion_control_design_tool/index.html. A link on the page provides access to a help guide providing detailed program input and output descriptions.
Fairchild Semiconductor,
www.fairchildsemi.com

Dual-axis accelerometer operates at 175°C

The dual-axis ADXL206 iMEMS (microelectromechanical-system) accelerometer has signal-conditioned analog-voltage outputs. The single-chip device measures both dynamic acceleration, such as tilt, and static acceleration, such as gravity, with a full-scale range of ±5g. The unit guarantees an operating-temperature range of –40 to +175°C and good overall stability, suiting geological downhole tools and other extremely high-temperature industrial applications. The ADXL206 has a typical noise floor of 110 µg/√Hz, allowing the resolution of signals of less than 1 mg, with 0.06° of inclination, in tilt-sensing applications using bandwidths narrower than 60 Hz. Users can select bandwidths of 0.5 Hz to 2.5 kHz to suit the application. The device comes in a 13×8×2-mm, eight-lead SBDIP and sells for $789 (1000).



Analog Devices Inc,
www.analog.com/ADXL206

STORAGE

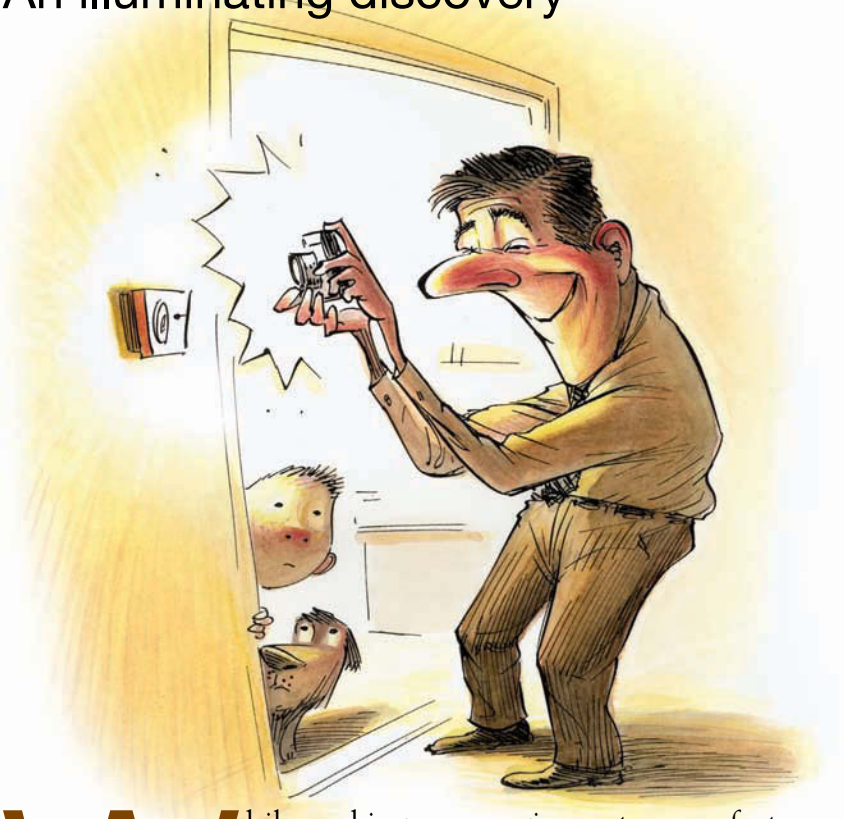
Drive has read speeds to 80 Mbytes/sec

The 128-Gbyte, 1.8-in. PATA ZIF solid-state drive offers sequential-read speeds as high as 80 Mbytes/sec and sequential-write speeds as high as 38 Mbytes/sec. The 70×54×5-mm device has the same dimensions as a 1.8-in. hard-disk drive and supports PIO Mode 6 and Ultra DMA Mode 6. The ZX N128G-PATAZIF-ZX family now includes 32-, 64-, and 128-Gbyte models. The 128-Gbyte drive is available from Amazon for $379.
Active Media Products,
http://activemp.com

Drive supports 6-Gbps SATA

The 64-Gbyte, C300 drive is backward-compatible with the 3-Gbps SATA interface and provides read speeds as high as 355 Mbytes/sec and write speeds as high as 75 Mbytes/sec. Available in a standard 2.5-in. form factor, the drive sells for $149.99.
Crucial, www.crucial.com

An illuminating discovery



While working as an engineer at a manufacturer of thermostats for residential applications, I had to change a display backlight from a fixed-current dim LED to a bright-blue PWM (pulse-width-modulator)-controlled LED. Months after we made the change and completed design reviews, production validation, and field tests, we started getting reports of lockups requiring a reset or power cycling to restore proper operation. We immediately reviewed the software, hardware, and minor changes that were on record.

Side-firing LEDs at the top of a 64×128 dot-matrix display illuminated the display module. A shaped and textured light pipe/reflector would reflect the light across the display. This reflector worked well but lost too much light, so we brightened the LEDs' output to achieve an impressive display. A recent change was a slightly lower-value 1% resistor for brighter display illumination.

The LEDs' PWM control allowed us to brighten them during button-pressing events, such as changing the temperature setting, and we could prolong the life of the LEDs by dimming them during idle periods. We even tweaked the design to let users adjust and smoothly change between the active and the idle brightness levels.

We found no problems with the units in user field tests or on the life test. We asked for feedback from dealers, installers, and users. Both a customer and an installer confirmed that the new thermostats failed during one of two modes: A freshly installed unit was either blinking a full-brightness "time-and-date-not-set" warning, or it was responding to a user's button press. The failure symptom was a blank display, but the temperature-control feature remained functional. We ruled out ESD (electrostatic discharge) because users were reporting blank displays that appeared even though no one had touched them or would appear several seconds after someone had pressed a button.

Staring at a disassembled LCD module, I was amazed at the fine lines of transparent indium-tin oxide on glass attaching 192 columns and rows to a driver/processor/RAM mounted as COG (chip on glass). The first time I had ever seen a bare microprocessor up close was in the 1980s when I desoldered the gold-plated metal lid from a ceramic, 40-pin DIP version of an RCA1802. Curious to see whether I had damaged the IC during disassembly, I plugged it into a working system socket. It powered up and ran without problems. I took a photo—using flash—of the working open-topped IC. The board immediately reset, blanking out the LED display and restarting. From this experience, I learned that every PN (positive/negative) junction can become a photodiode, attempting to generate voltage and current. Exposing thousands of photodiodes to bright flashes of light disrupts the IC-logic processes and trips up the system. This IC should definitely remain in the dark.

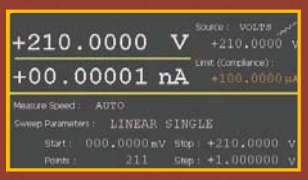
Returning to the problem at hand, I performed a series of tests using photo flash, a brighter backlight, a stroboscope, and a tactical flashlight. The results showed the same problem. To fix it, I placed black electrical tape on the glass opposite the IC to shield it from the light and reduce the sensitivity, even to light injected from the user. We explained the problem to the module manufacturer and fixed the problem. Users could get a replacement or simply keep the brightness at eight instead of 10.

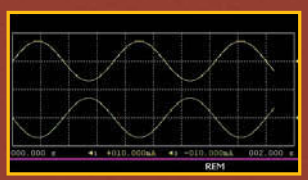
Within six months, several LCD-module makers had added black tape opposite the COG-driver IC and opaque sealant atop the IC. One of their IC data sheets warned: "Do not expose to light." EDN

George Catlin is a senior design engineer at Exceptional Innovation (Westerville, OH).

DANIEL VASCONCELLOS

Choose a bench-top SMU that's clearly more efficient.





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Agilent Technologies

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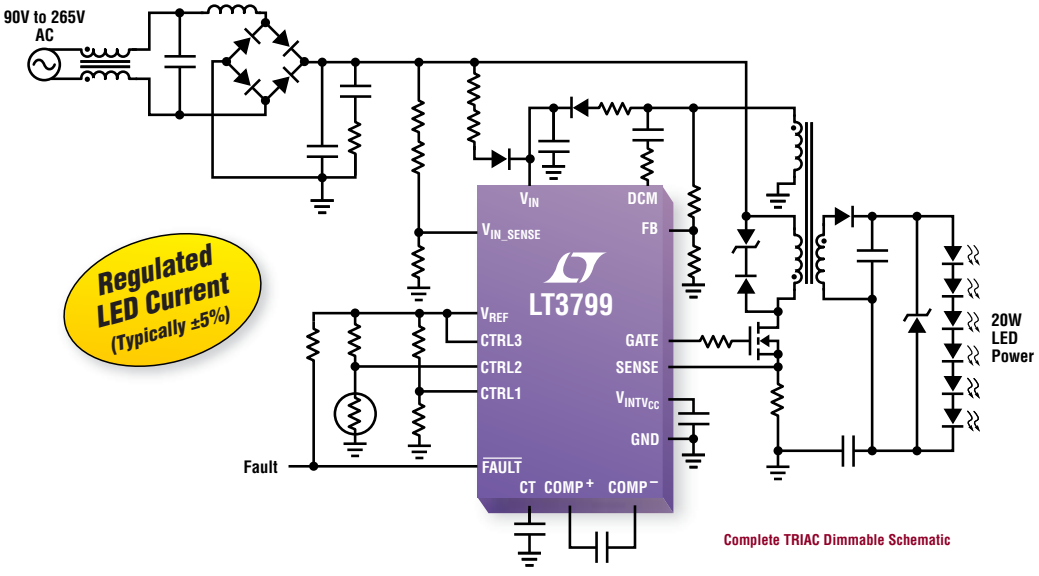

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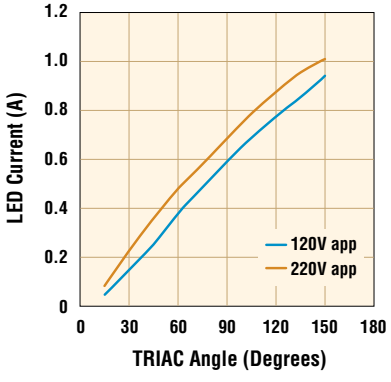
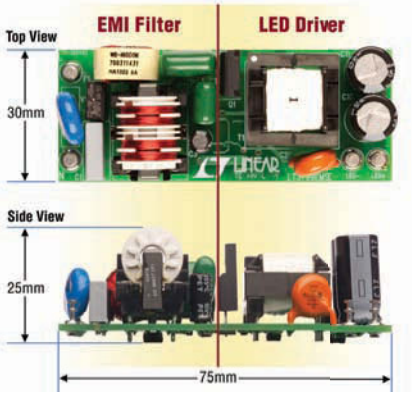
LED Current vs TRIAC Angle



LT3799 Demo Board (25W)



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